

CHARACTERIZATION OF  
ELECTRICAL CONTACTS FOR  
PHASE CHANGE MEMORY CELLS

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Cover image: Water drops falling onto water. This illustrates charge carriers flowing from the phase change materials into the metal electrode at the contact.

# CHARACTERIZATION OF ELECTRICAL CONTACTS FOR PHASE CHANGE MEMORY CELLS

DISSERTATION

to obtain  
the degree of doctor at the University of Twente,  
on the authority of the rector magnificus,  
prof.dr. H. Brinksma,  
on account of the decision of the graduation committee,  
to be publicly defended  
on Wednesday the 28<sup>th</sup> of September 2011 at 16:45

by

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Printed in The Netherlands

*To the memories of my grandfather V. M. John*



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*Phase change random access memory is an emerging candidate as a potential replacement for transistor based flash memories. The objective of this work is to characterize and model the electrical contacts present in these memory cells. The contact properties have a significant influence on the electrical performance, scaling and reliability of these devices.*

*This chapter begins with an introduction to the different types of emerging semiconductor memory technologies and phase change random access memory in detail. The significance of this research work for phase change memories is discussed in the second session. The organization of this thesis dealing with the characterization of the different aspects of these contacts is also presented.*

## 1.1 Semiconductor memory technology

Semiconductor memory is an electronic digital data storage device fabricated in a complementary metal oxide semiconductor (CMOS) based circuitry [1][2]. A type of non-volatile memory that can be erased in large blocks is called the flash memory, which drives the scaling in the memory industry [3]. Flash memories are being used in cellular phones, digital cameras, audio players, universal serial bus (USB) memories, smart cards and many other devices [4]. The advances in consumer electronics and mobile devices demand an increasing requirement for a non-volatile memory with improved performance and better opportunities for dimensional scaling. This leads to the quest for a unified scalable memory for future integrated circuits that combines the required properties of several memory technologies [5][6][2]. They should be scalable and at the same time have the lowest cost per bit. It should have the non-volatile nature of flash, endurance (read and write performance) and speed of DRAM and SRAM. In addition, this memory technology should be compatible with embedded (CMOS technology) and stand alone application with multibit-storage and 3D integration potential. Several novel memory concepts have been researched over the past years to qualify these requirements. The latest classification of present and future semiconductor memory devices as projected by the International Technology Roadmap for Semiconductors (ITRS) is given in Fig. 1.1 [2]:

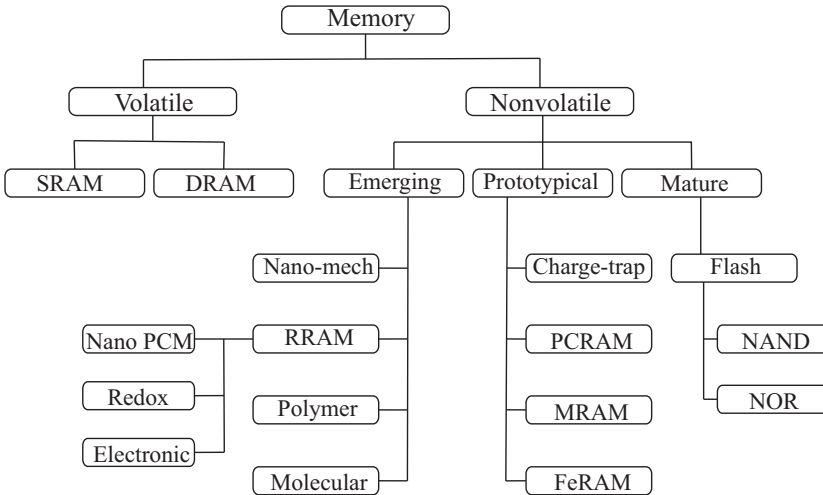


Figure 1.1: Classification of semiconductor memory technology by ITRS.

For the short term (2016-2021 time frame) phase change random access memory (PCRAM), magnetic random access memory (MRAM) and ferroelectric random access memory (FeRAM) are being considered as a potential replacement for present day flash memories.

## 1.2 Phase change random access memory

In phase change memory cells, information is stored as the amorphous or crystalline state of the integrated phase change material [7][8]. These materials are compounds or alloys which contain one element from group VI of the periodic table. They are widely used as the active material in compact disc-rewritable (CD-RW) and digital versatile disc-rewritable (DVD-RW), where the optical reflectivity difference of the two states is used to store information [9]. In this case programming and read out is achieved by laser pulse operation. In PCRAM cells the difference in resistance between the states is employed to achieve the memory functionality. The crystalline state has a two to three orders of magnitude lower electrical resistivity than the amorphous state. Switching is achieved by electrical pulse operation. In this study, the commonly used materials based on antimony (Sb) and tellurium (Te),  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  and doped- $\text{Sb}_2\text{Te}$ , are investigated. Electrically controlled switching of PCM was first reported by Ovshinsky in 1968 [10]. Later the first 256 bit phase change memory array was demonstrated in 1970 by R. G Neale, D. L. Nelson and Gordon E. Moore [11]. This memory cell consisted of a PCM resistive storage element in series with a silicon based  $p$ - $n$  diode as an access device. Even though the concept was developed and prototypical devices were fabricated, the memory industry did not follow the phase change memory technology because of the large power required to program these cells. The reset energy at that time was  $25 \mu\text{J}/\text{bit}$ . This energy required to program depends on the volume of PCM in the cell.

As the semiconductor industry faithfully followed Moore's law<sup>1</sup>, lithographic tools were developed that can define smaller feature sizes. With this shrink in the feature size, the volume of the material in the PCRAM cell decreased with cubic progression. Reaching the 180 nm technology node, the power required to program a phase change memory cell is demonstrated to be feasible to be used in electronic devices [8]. This power consumption for PCRAM cell will decrease as the device size is further scaled down [13]. The write energy is now in the range of 5 pJ/bit [2].

An embedded PCRAM cell consists of a thin-film PCM layer integrated in the metallization level of an integrated circuit in combination with an access device. Different integration schemes have been proposed [3][8][14] following the original Ovonic Unified Memory (OUM) concept [15]. The cell architecture introduced by NXP Semiconductors is the *line* cell concept. Here a thin line of PCM is placed between two metal electrode contacts [5]. A top-view transmission electron microscope (TEM) image of such a line cell switched to the amorphous state is shown in Fig. 1.2(a). The memory storage or programmable part of the PCM is the line that is switched between amorphous and crystalline states [7]. The schematic cross section of which is shown in Fig. 1.2(b).

Programming operation of the memory cell from high resistance (Fig. 1.2(a))

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<sup>1</sup>The number of devices in a given chip area roughly doubles every year [12].

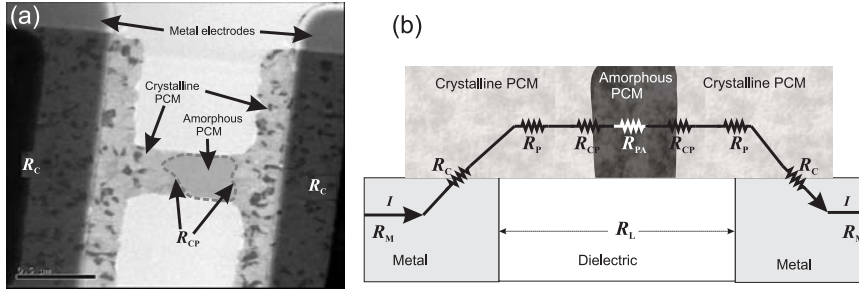


Figure 1.2: (a) Top-view TEM image of the PCM line cell. (b) Schematic cross section of the line showing the switching region, including the electrical schematic.

to low resistance (set operation) is achieved by threshold switching ( $V_{TH}$ ) and subsequent thermal annealing (typically at 250 °C of the disordered amorphous material part into the ordered crystalline state [8][5]). Thermal steps are achieved by Joule heating using electrical pulses from the accompanying transistor. Switching of the memory cell from low resistance (crystalline) to high resistance (amorphous) (reset operation) involves the heating of the PCM by higher electrical pulses above the melting point at typically 650 °C and cooling it quickly (quenching). The material remains in the amorphous melt-quenched state. Set, reset and read out are done by the same transistor using different electrical pulses.

The resistance of the cell in the set (crystalline) state  $R_{set}$  is determined by the PCM line resistance ( $R_L$ ), contact resistance ( $R_C$ ) and the metal resistance ( $R_M$ ), as depicted in Fig. 1.2(b). In the reset state, the resistance of the line cell  $R_{reset}$  is mainly determined by the amorphous PCM present in the cell. In other cell configurations also the contact resistance of metal electrodes to amorphous PCM is involved.

### 1.3 Scope of this work

This thesis deals with the characterization of electrical contacts for phase change memory cells. Electrical contacts are an integral part of the phase change memory cell. The nature is expressed in terms of contact resistance  $R_C$  and specific contact resistance  $\rho_c$ . As the critical feature size  $F$  of semiconductor devices scales down into the (sub micrometer) nanometer regime, the physical size of electrical contacts in the device also decreases. This is because the scaling of the contact resistance approaches  $F^{-2}$  for small contacts [16]. Hence the relative contribution of the contact resistance increases more rapidly than the device resistance. In the case of a phase change memory cell,  $\rho_c$  of the electrode to crystalline PCM is approximately  $7 \times 10^{-8} \Omega \cdot \text{cm}^2$  (as will be shown in the following chapters). This means that a square contact of 100 nm  $\times$  100 nm results in a  $R_C$  of 700  $\Omega$  per contact. This is a significant value when compared to the PCM line

resistance  $R_L$ , which is adjusted to  $2\text{ k}\Omega$  by the geometry of the PCM layer. During reset operation, the impedance of the access device should be matched with the set resistance of the cell  $R_{\text{set}}$ , for optimum power transfer. This includes the resistance of the crystalline line to be amorphized  $R_L$  and the contact resistance  $R_C$ , that acts as a parasitic resistance. During set operation,  $V_{\text{TH}}$  depends on the voltage across the amorphous region. For other technology nodes the resistance of the line cell should be adjusted to the accompanying transistor. This includes the geometry and the material of the line cell  $R_L$  itself and the contact resistance  $R_C$ . With the knowledge of  $\rho_c$ , the contacts in a PCRAM cell can be engineered for optimum device performance, not to be a limiting parameter for the performance of next generation CMOS devices. For other than the line cell configurations, the  $R_C$  for electrode to amorphous PCM are also of importance [17]. Moreover the influence of thin (down to 5 nm) PCM layers and the behavior under high frequencies (user) conditions further improve the understanding of the memory cells.

Although important for electrical performance optimization and scaling of phase change memories, very little attempts have been reported to understand the electrode to PCM contact properties [17][18]. The aim of this work is to gain a microscopic and macroscopic understanding of electrode to PCM contacts. As the PCM technology scales in dimension and incorporate different material and device architectures, improvement in performance demands the understanding of the PCM and its contacts. In this thesis the following subjects will be discussed:

- What measurement structures are suitable to characterize electrode to PCM contacts?
- What contact resistivity values are achievable for PCRAM cells?
- What is the charge transport mechanism at the electrode to PCM interface?
- What is the contact resistance value at the operating frequency of a PCRAM cell?
- What is the influence of parasitic current paths in test structures on the measured values?

## 1.4 Outline of the thesis

In chapter 2 contact resistance and different measurement structures used in this research are introduced. Different types of interfacial charge transport mechanisms are briefly reviewed from a metal to semiconductor contact perspective. Measurements presented in the following chapters on metal to PCM contacts reveal similar properties.

In chapter 3 the different material parameters of the PCM like resistivity, mobility, carrier concentration and optical band gap are determined from electrical,

optical and Hall effect measurements. The knowledge of these parameters is essential along with the contact resistance values to establish the electrical conduction mechanisms at the contact.

In chapter 4 the  $\rho_c$  extracted for TiW to doped-Sb<sub>2</sub>Te and Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> from two different measurement structures are compared. In the amorphous state of the PCM, these contacts exhibit a polarity dependence and temperature dependence. Based on the measurements with different electrodes and using a metal to semiconductor model, the interface barrier creation and charge transport mechanism at the contact are modeled with the presence of donor and acceptor states in the PCM. In the last part of this chapter the extracted  $\rho_c$  values for different thicknesses of doped-Sb<sub>2</sub>Te layers are reported.

In chapter 5 a modified test structure and a novel data extraction procedure is presented that is suitable for electrical contact interface characterization with frequency. The relevance of high frequency (HF) measurements, design criterion and the steps involved in the fabrication of these test structures are described in the first part of this chapter. Measurements were performed on two different test structures up to 4 GHz. Based on these measurements, the contact is modeled with a resistance capacitance network. This method can separate the interface resistance from the interface capacitance values.

In chapter 6 the influence of parasitic current paths in the test structures on measured resistance is discussed. They lead to additional potential drops and higher measured resistance values. During patterning of the PCM layer, conducting re-deposited sidewalls are formed around the etched layer. In the first part, the presence of re-deposited sidewalls is experimentally characterized by resistance measurements on Van der Pauw structures. The impact of the formed sidewalls on contact resistance measurements and data extraction from these structures is shown. In the reset state of the PCRAM cell, in addition to the electrode to PCM interface, crystalline PCM to amorphous PCM interfaces are also present. In the second part of this chapter, test structures are presented to characterize the interfaces between crystalline and amorphous PCM. Attempts to characterize these interfaces were hindered by the formation of a non-uniform interface due to re-deposited residues and partial crystallization of the amorphous PCM. Details of these experiments with TEM evidence are presented.

Finally in the last chapter, the results are summarized from a PCRAM line cell perspective.



## Contact resistance methodology

*This chapter introduces the contact resistance and the different measurement structures that are suitable for contact resistance characterization. In the first part, the contact resistance in a PCRAM cell and the parameters that determine the nature of this interface are presented. In section 2, interfacial barrier creation and the possible charge transport mechanisms at a metal to semiconductor is briefly discussed. Our results in Chapter 4 indicate that metal to phase change material contacts show similar properties as metal to semiconductor contacts. To cross the interface charge carriers have to overcome a potential barrier which creates an interfacial potential. Contact characterization is essentially the determination of this interfacial potential drop, and it is expressed in terms of contact resistance and specific contact resistance. Measurement structures that are suitable to characterize these interfaces are Kelvin resistor structures and Transfer Length Method structures. The theory and data extraction procedure from these test structures are discussed in section 3. In an electronic device during operation the memory cells will be accessed at a certain speed. Hence it is relevant to know the contact resistance value at its operating frequency. In the following section a modified test structure is presented which is suitable for contact resistance measurements with frequency. Each test structure has its own design rules, measurement range and limits. This knowledge is essential for proper selection of a test structure for accurate extraction of specific contact resistance values. This is discussed in the subsequent section.*

## 2.1 Contact resistance

In micro/nano electronic devices, a *contact* refers to the metallization layer applied to have a good electrical and physical contact with the functional layers in a (semiconductor) device. Through these contacts the current enters and leaves the device. Depending on the pattern of current flow to these contacts, they are classified into [19];

- Vertical contacts: The current flows vertically to the contact having a uniform current distribution.
- Horizontal contact: The current flows laterally to the contact. This leads to current crowding effects at the contact edges.

A PCRAM *line* cell as shown in Fig. 1.2 consists of a line of phase change material contacted with metal electrodes on both ends. The schematic cross section of this cell with a current,  $I$  flowing from A to B is shown in Fig. 2.1. The contacts formed in these cells are horizontal contacts. The total resistance

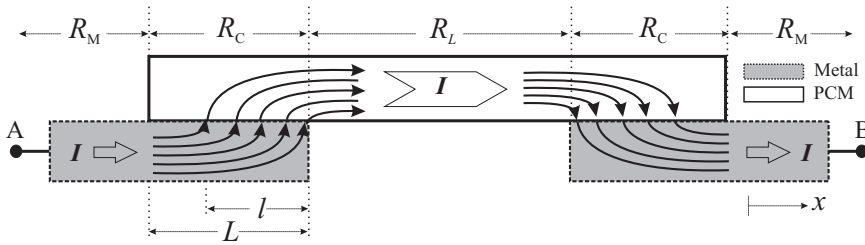


Figure 2.1: Schematic cross section of a PCRAM line cell with the pattern of current flow.

between terminals A and B is then represented as:

$$R_{AB} = 2R_M + R_L + 2R_C \quad (2.1)$$

The value of the resistance of the metal electrode  $R_M$  and resistance of the PCM between the metal electrodes  $R_L$  is determined from the geometry of the cell and the sheet resistance values of metal and PCM.  $R_C$ , the total resistance encountered as the current is forced from metal electrode to the PCM, can be determined from measurements on dedicated test structures.  $R_C$  depends on [20][21]:

- *Physical properties of the materials:* At the contact in a thin surface layer of the materials, the charge carrier density differs from that of the bulk. This is due to the difference in the work function of the two materials at the contact or due to the presence of surface states.

- *Process limiting factors*: This could be due to the presence of a thin layer of conducting or non-conducting foreign matter or oxidation of the material or a chemical reaction at the interface.
- *Current crowding*: Due to geometrical effects, the presence of a contact alters the electric field and hence the current distribution in the vicinity of the contact. This change in current distribution introduces additional resistance to current flow.

The parameter describing the physical properties of the interface is defined as the intrinsic resistivity,  $\rho_i$ . The contact resistance ( $R_C$ ) includes the contribution of intrinsic resistivity  $\rho_i$ , the portion of the metal below the interface and PCM above the interface, current crowding effects and the presence of any interfacial layer at the contact. In a real contact these possible contributions occur simultaneously<sup>1</sup> [20][21][23]. This leads to the term contact resistivity or specific contact resistance  $\rho_c$ . This value is related to  $R_C$  with the effective contact area (see eq. 2.9). Thus the electrical nature of a contact is characterized by contact resistance,  $R_C(\Omega)$  and specific contact resistance,  $\rho_c(\Omega.cm^2)$ . When evaluated at zero bias,  $\rho_c$  is an important figure of merit for transport characteristics at the barrier; defined as [24]:(Derivation in appendix A1)

$$\rho_c = \left( \frac{\partial J}{\partial V} \right)_{V=0}^{-1} \quad (2.2)$$

$\rho_c$  is considered as the figure of merit in case of *ohmic* contacts. It is independent of contact area and hence it is a convenient parameter to compare contacts of different size. This  $\rho_c$  is used in this research.

## 2.2 Current transport at the interface

The general theory of equilibria [25] states that when two electronic conductors are in contact and in thermal equilibrium, the electrochemical potentials (Fermi level) must be the same in both conductors. Charge transfer takes place through the interface to bring the two Fermi energies into alignment. This creates an opposing dipole that prevents further charge transfer and the contact potential developed depends on the work function difference of the two materials. A space charge region is created in the semiconductor material close to the interface, which is depleted of mobile charge carriers. The charge on the surface of the metal is within the Thomas-Fermi Screening length ( $\approx 0.05$  nm) [26]. The extent of the space charge region into the semiconductor depends on the doping level. The existence of a barrier to charge carriers at the metal-semiconductor interface was independently proposed by Schottky [27][28][29] and Mott [30]. This charge

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<sup>1</sup>For metal to metal contacts treated by Holm [22] contact resistivity is the constriction resistance, where the interface and the bulk effects are not separated.

transfers across a metal to semiconductor (or a dielectric) interface, according to the Schottky model is governed by a barrier height ( $\phi_b$ ). This is the energy difference between the Fermi level and the majority carrier band edge at the interface, which is valence band maximum for  $p$ -type materials and conduction band minimum for  $n$ -type materials. For an ideal metal to semiconductor interface, i.e. one in which the interface is inert and without surface or induced interface states in the semiconductor, the barrier height measured relative to the Fermi level for metal to  $n$ -type ( $\phi_{bn}$ ) and  $p$ -type ( $\phi_{bp}$ ) semiconductors is given by [31]:

$$q\phi_{bn} = \Phi_M - q\chi \quad \& \quad q\phi_{bp} = E_g + q\chi - \Phi_M \quad (2.3)$$

where,  $\chi$  is the electron affinity of the semiconductor measured from the bottom of the conduction band to the vacuum level and  $E_g$  is the semiconductor band gap. This is referred as Schottky-Mott limit, by which the barrier height is determined by the metal work function<sup>2</sup>( $\Phi_M$ ).

The current transport at a metal-semiconductor interface is mainly determined by majority carriers crossing the barrier. The total current through the interface at equilibrium condition constitutes of a thermionic emission component and a tunneling component. The relative magnitude of these two cases at an interface depends on the temperature  $T$  and carrier concentration  $N_C$ . The carrier concentration at which the conduction mechanism at the contact changes from one to other is based on the characteristic energy  $E_{00}$ , a material constant that determines the tunneling probability.  $E_{00}$  is defined as [32]:

$$E_{00} = \frac{qh_p}{4\pi} \sqrt{\frac{N_C}{m^*\epsilon}} = 18.5 \times 10^{-12} \sqrt{\frac{N_C}{(m^*/m)\epsilon_r}} \quad (2.4)$$

where,  $h_p$  is the Planck's constant,  $q$  is the electronic charge,  $m^*$  is the effective mass of the tunneling electron,  $m$  is the free electron mass, and  $\epsilon_r$  is the dielectric constant of the semiconductor. The ratio  $k_bT/E_{00}$  is a measure of thermionic process in relation to tunneling. In the case of materials with [33];

- low carrier concentration,  $k_bT \gg E_{00}$  and thermionic emission (TE) process dominates the current transport through the interface.
- large carrier concentration,  $k_bT \ll E_{00}$  and current transport is by tunneling or field emission (FE) through the barrier.
- In between,  $k_bT \approx E_{00}$ , current flows due to electrons with energy tunneling through the mid section of the potential barrier. This is called thermionic field emission (TFE).

---

<sup>2</sup>Work function  $\Phi_M$  is the energy difference between the vacuum energy level and the Fermi energy level. Vacuum energy level represents the energy at which the electron can be free of the material and could be emitted away from the solid.  $\Phi_M$  is related to the potential  $\phi_M$  by the relation  $\Phi_M = q\phi_M$

The current transport at a contact is primarily described by TE theory if the barrier height is larger than  $k_bT$ , and the carriers are thermally excited over the barrier. Assuming Maxwell-Boltzmann approximation, the current density ( $J$ ) at the metal to semiconductor junction, without image force lowering is expressed as [31]:

$$J = \left[ A^* T^2 \exp\left(\frac{-q\phi_b}{k_bT}\right) \right] \left[ \exp\left(\frac{qV_a}{k_bT}\right) - 1 \right] \quad (2.5)$$

The first term in this is saturation current density  $J_{ST}$ , which is dependent on the zero bias barrier height. Using eq. 2.2,  $\rho_c$  at zero bias is calculated for thermionic emission model as [24]:

$$\rho_c = \frac{k_b}{qA^*T} \exp\left(\frac{-q\phi_b}{k_bT}\right) \quad (2.6)$$

As evident from this equation for TE model  $\rho_c$  decreases exponentially with decreasing  $\phi_b$  and increasing temperature. At the same time  $\rho_c$  is independent of  $N_C$  and voltage bias (unless image force lowering is considered which will lowers  $\phi_b$ ).

At high  $N_C$  the extent of the space charge region in the semiconductor will also be small such that quantum mechanical tunneling of the charge carriers takes place through the interface. In this case the current through the interface is proportional to the quantum transmission coefficient multiplied by the occupation probability. With current transport dominated by tunneling,  $\rho_c$  is expressed as [31]:

$$\rho_c = \exp\left(\frac{q\phi_b}{E_{00}}\right) = \exp\left[\frac{4\pi\sqrt{\epsilon m^*}}{h_p} \left(\frac{\phi_b}{\sqrt{N_C}}\right)\right] \quad (2.7)$$

In the tunneling regime  $\rho_c$  is independent of temperature, but depends strongly on  $N_C$  and tunneling effective mass. The tunneling probability increases with  $N_C$ , making the potential barrier thinner and easier to tunnel through.

Thermionic field emission (TFE) is the situation that bridges the two limits. In this case the thermally excited carriers reach an energy where the barrier is reasonably narrow for tunneling to occur. With TFE,  $\rho_c$  is expressed as [33]:

$$\rho_c = \exp\left(\frac{q\phi_b}{E_{00} \coth\left(\frac{E_{00}}{k_bT}\right)}\right) = \exp\left[\frac{4\pi\sqrt{\epsilon m^*}}{h_p} \left(\frac{\phi_b}{\sqrt{N_C} \coth\left(\frac{E_{00}}{k_bT}\right)}\right)\right] \quad (2.8)$$

In this case,  $\rho_c$  depends on temperature,  $N_C$ , tunneling effective mass, and on the  $\phi_b$ .

A good *ohmic* contact has no potential barrier at the interface, hence  $\rho_c$  should be sufficiently small to exhibit a linear or quasi-linear current-voltage ( $I$ - $V$ ) characteristic. For devices, a contact is also considered *ohmic*, if the voltage drop across the contact is small compared to the voltage drop across the active region of the device [34]. In the case of dedicated test structures, metal-semiconductor contacts with a high carrier concentration in the semiconductor, the depletion

region width becomes small, such that the electrons can tunnel through the barrier in addition to thermionic emission process [35]. This added component of tunneling current reduces the voltage across the contacts, resulting in an *ohmic* contact [33]. Similar case exists for electrode to crystalline PCM contacts. Ideal interfaces are homogeneous, intimate, abrupt, and free from any structural or chemical defects. Our measurements indicated that structural defects exist in the PCM at the interface. This leads to deviation of the metal to PCM interface properties from an ideal metal to semiconductor interface. These non idealities will be treated in the subsequent chapters.

## 2.3 DC contact resistance measurement structures

Metal-semiconductor contacts had been identified and researched for the past two centuries are now commonly referred as Schottky-barrier devices in honour of Walter H. Schottky [36] who formulated the first acceptable theory of rectification at these contacts [27][28][29]. For electrical conduction at these contacts charge carriers need to pass the potential barrier at the interface. Depending on the nature of the interface, as described in the previous section this results in an interfacial potential drop. Characterization of the contacts is essentially determination of this interfacial potential drop. This interfacial potential drop is separated from the potential drop in the device and is expressed as contact resistance,  $R_C$ . This section describes the test structures suitable for interface characterization, and the data extraction procedure to obtain  $\rho_c$  values from these structures. Direct measurement of individual contact resistance is possible using a four-terminal Kelvin resistor structure [37]. A technique to measure planar contact resistance associated with metal-semiconductor interface was developed by Shockley [38]. In this approach, current is constrained to flow from one metal contact to the semiconductor, through which it flows for a length and then enters into the second metal contact. From the associated voltage drop and knowledge of the sheet resistance  $R_{SH}$  of the semiconductor layer the contact resistance is estimated. A model describing planar contacts on monolithic structure was developed by Kennedy and Murley [39]. This model shows large current crowding effects at the contacts, which was refined independently using transmission line equations by Berger [40] and Murrmann and Windmann [41] [42][43]. When the current flows from PCM to metal or vice versa at the contact it encounters  $R_{SH}$  and  $\rho_c$ , choosing the path of least resistance. This leads to current crowding at the contact which results in a suitable parameter, the transfer length  $l$ , from which the  $\rho_c$  is extracted. The  $\rho_c$  extraction model based on this parameter is known as the transfer length method (TLM). In the case of the measurement structures based on this model, contact resistance determination deals with a difference rather than absolute values. Various other two terminal methods like twin contact method, extrapolation method, differential method and contact chains or contact strings [20][44] also exist for contact resistance determination. In this work we focus on

Kelvin resistor and transfer length method structures.

### 2.3.1 Kelvin resistor structures

The Kelvin resistor is a planar structure suitable for interfacial contact resistance measurements with minimum parasitic resistance interference [37]. In the Kelvin measurement, the current and voltage at the contact are measured using a four terminal force-sense configuration. The schematic of a Kelvin resistor structure and its cross section along the contact area is shown in Fig. 2.2. The structure consists of a metal segment and a PCM segment, with an overlap area ( $A$ ) which serves as the contact.

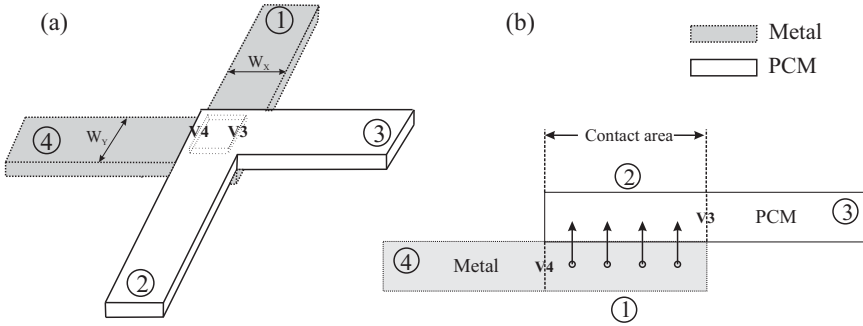


Figure 2.2: Schematic representation (not to scale) of the Kelvin resistor structure (a), cross-section (b) along the contact region.

To measure the metal to PCM contact resistance, a current is forced from the metal to PCM (1 to 2) and the voltage is measured orthogonal to the direction of current flow (3 and 4). This allows measurement of the average voltage,  $V$  (is  $V_4 - V_3$ ) at the contact, from which the contact resistance ( $R_C$ ) is calculated. This four terminal measurement avoids the probe to contact pad resistance and the resistance of the current and voltage taps up to the contact region from the measured resistance. The specific contact resistance,  $\rho_c$  is then calculated from  $R_C$  as:

$$\rho_c [\Omega.\text{cm}^2] = R_C \times A \quad (2.9)$$

Misalignment of the layers at the contact could lead to a contact width which is different from the tap width. This results in a resistive drop due to current flow in the periphery of the contact area. This lateral current crowding strongly affects the measurement accuracy of  $\rho_c$  which is appreciably visible in the range lower than  $10^{-6} \Omega.\text{cm}^2$  [45][46]. In this case the extracted  $\rho_c$  using eq. 2.9 will be over estimated due to the current crowding effects around the contact. Two-dimensional numerical simulations were required to extract  $\rho_c$ , taking into account the current crowding in the overlap region around the contact area [45][47][48]. This misalignment tolerance can be avoided by fabricating the same structures

with a defined contact area ( $A$ ) in the dielectric surrounded by a well defined overlap region ( $\delta$ ). These structures are basically the same Kelvin resistor structures. They are known as cross-bridge Kelvin resistor (CBKR) structures [48]. The SEM image of such a CBKR structure with a contact area ( $A$ ) and an overlap length ( $\delta$ ) is shown in Fig. 2.3(a), the schematic cross-section is shown in Fig. 2.3(b). As the current flows through these structures, it creates a potential drop in the interfacial contact region as well as in the  $\delta$  region. The measured resistance ( $R_K$ ) consist of two components; one due to the voltage drop at the actual contact,  $R_C$ , and the other due to the voltage drop due to current flow around the contact in the  $\delta$  region,  $R_D$ . The first component,  $R_C$  depends on  $\rho_c$  the contact area  $A$ , while the second component,  $R_D$  depends on the geometry of the structure.

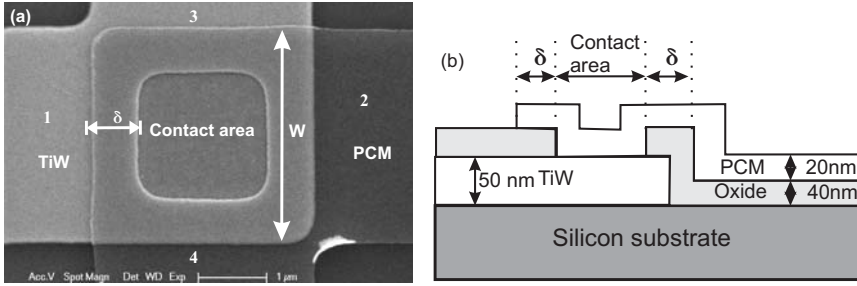


Figure 2.3: CBKR structure showing the metal (TiW) and the PCM segments (a) Top view SEM image and (b) cross section view. The contact area and overlap length ( $\delta$ ) between the two layers is also shown.

The change in  $R_K$  of the CBKR structures with  $\delta$ , for given contact area is shown in Fig. 2.4. To determine  $\rho_c$  accurately from these CBKR measurements, the contribution of  $R_D$  needs to be eliminated from  $R_K$ . The geometrical dependence of the overlap region to the total measured resistance is given by [49]:

$$R_K = R_C + R_D = \frac{\rho_c}{A} + \frac{4R_{SH}\delta^2}{3W^2} \left[ 1 + \frac{\delta}{2(W - \delta)} \right] \quad (2.10)$$

Using eq. 2.10,  $\rho_c$  is extracted numerically or graphically with the knowledge of the geometrical parameters of the CBKR structure and  $R_{SH}$  of the PCM layer.

### 2.3.2 Transfer Length Method (TLM) structures

In the case of a lateral contact a current  $I$ , travelling from the metal into the PCM will generate a voltage drop at the metal to PCM interface. At each point at the contact the current branches through the contact and through the PCM. This is schematically shown in Fig. 2.5. The potential distribution at the contact is determined from  $R_{SH}$  and  $\rho_c$ , which is electrically modeled as a resistive network



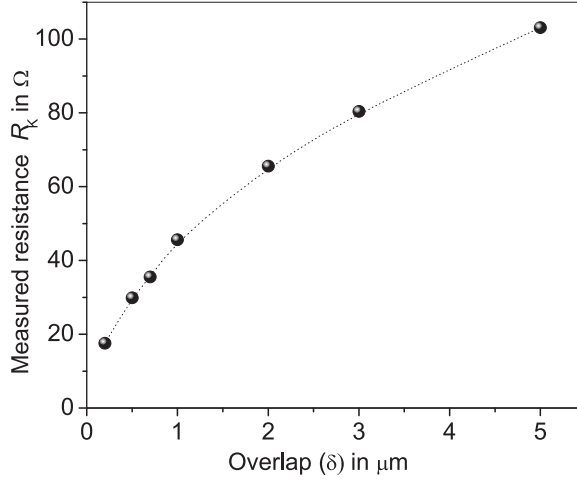


Figure 2.4: Change in  $R_K$  with  $\delta$  for a fixed contact area.

[50][44]. The current in the PCM decreases exponentially with the distance. The related voltage distribution under the contacts is given by [42][34]:

$$V(x) = V_0 \frac{\cosh[(L-x)/l]}{\sinh(L/l)} \approx V_0 \exp(-x/l) \quad (2.11)$$

Where  $V_0$  is the voltage at the leading edge of the contact,  $L$  is the length of the contact,  $l$  is the contact current transfer length and  $x$  indicates the direction of current flow.

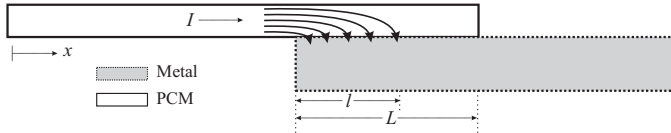


Figure 2.5: Current transfer at a metal to PCM interface showing current crowding at the leading edge of the contact.

The contact parameters can be extracted by solving the differential current and the voltage equations describing the transmission line equivalent circuit of the contact [41][40][51]. The sheet resistance of the metal and the PCM and the interfacial resistance at the contact region have to be taken into account [42]. Assuming sheet resistance of the PCM much larger than that of the metal, the characteristic length of current transfer  $l$  at the contact is defined as [52]:

$$l = \sqrt{\frac{\rho_c}{R_{SH}}} \quad (2.12)$$

This is also defined as the "1/e" distance of the voltage curve represented by eq. 2.11 [44]. For contacts with  $L \gg l$ , all the current will be transferred over a distance  $L \gg 5l$  [42][39]. In TLM structures, the method to extract the contact resistivity is based on determining the value of  $l$ .  $\rho_c$  is then extracted using eq. 2.12. Different layouts for TLM structures have been developed: linear-TLM structure [41][40][53], circular-TLM structure [54], and Scott-TLM structures [55].

### Linear TLM

The linear-TLM structure consists of identical contacts with different spacing  $d_i$  (see Fig. 2.6). To determine the contact parameters, resistance measurements

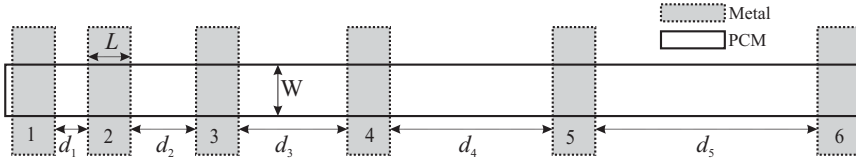


Figure 2.6: Schematic layout of a liner-TLM structure.

are performed between adjacent metal pads. A current is forced from one metal pad through the PCM layer to the other metal pad using a pair of probes. The corresponding voltage drop is measured using a second pair of probes. Assuming an identical contact resistance for all contacts, the total measured resistance ( $R_{Ti}$ ) between two metal pads is expressed as [50]: (derivation is presented in Appendix A2)

$$R_{Ti} = \underbrace{R_{SH} \left( \frac{d_i}{W} \right)}_{R_{PCM}} + \underbrace{\left( \frac{2l}{W} \right) R_{SH} \coth \left( \frac{L}{l} \right)}_{R_{contact}} \quad (2.13)$$

The sheet resistance of the metal is assumed to be negligible. If the length of the contact  $L$  is considerably larger than the transfer length  $l$ , then the equation 2.13 can be simplified to [19]:

$$R_{Ti} \approx \frac{R_{SH} d_i}{W} + \frac{2R_{SH} l}{W} = \frac{R_{SH} d_i}{W} + 2R_C \quad (2.14)$$

For two metal pads with spacing  $d_1$  and  $d_2$ , the measured resistance is  $R_{T1}$  and  $R_{T2}$ . Using eq. 2.14,  $R_C$  and  $R_{SH}$  of PCM can be calculated as:

$$R_C = \frac{R_{T2} R_1 - R_{T1} R_2}{2(d_1 - d_2)} \quad (2.15)$$

$$R_{SH} = (R_{T1} - R_{T2}) \frac{W}{(d_1 - d_2)} \quad (2.16)$$

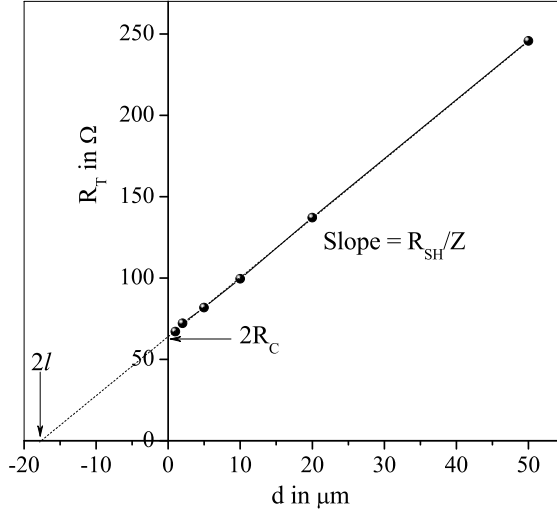


Figure 2.7: Measured resistance ( $R_T$ ) with gap spacing  $d$  for linear-TLM. Estimation of  $l$ ,  $R_C$ , and  $R_{SH}$  is also shown.

The resistance measured for different spacing and can be plotted versus  $d$  as shown in Fig. 2.7. This is essentially the plot of the linear relation as is in eq. 2.14. The contact parameters can also be extracted from the  $l$  which can be obtained graphically from this plot [53].  $R_{SH}$  is the slope of the curve times width of PCM layer,  $W$ . From the intercept at  $d = 0$ , two times the contact resistance ( $R_T = 2R_C$ ) can be obtained and the intercept at  $R_T = 0$  gives two times the contact transfer length ( $-d = 2l$ ). From  $l$ , the  $\rho_c$  is extracted using eq. 2.12.

### Circular TLM

The circular-TLM structure is basically the same as the linear-TLM in terms of measurement and contact parameter extraction, but with a different layout. These structures consist of circular metal contacts with ring shaped spacing  $d_i$  [54]. A SEM image of a circular-TLM test structure with an inner circular contact pad of diameter,  $D$  and a ring shaped spacing  $d$  with the outer metal contact is shown in Fig. 2.8(a). Similar structures are available with different spacing,  $d$  (see Fig. 2.8 (b)).

For electrical contact resistance measurements a current is forced from the inner to the outer circular metal contact and the voltage drop between metal contacts is measured. Measurements on circular-TLM structures with different gaps result in different resistance values. The total measured resistance,  $R_T$  between the inner and outer contact as derived from transmission line equation

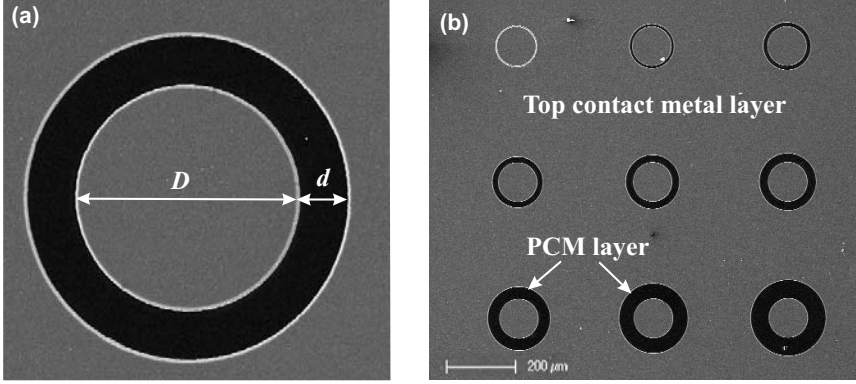


Figure 2.8: Layout of (a) an individual circular-TLM structure, (b) circular-TLM structures used for measurements.

is given as [56][57][58]:

$$R_{Ti} = \frac{R_{SH}}{2\pi} \left[ \frac{l}{L_d - d_i} + \frac{l}{L_d} + \ln \left( \frac{L_d}{L_d - d_i} \right) \right] \quad (2.17)$$

where  $L_d$  is  $(D/2) + d$ , and  $R_{SH}$  is the sheet resistance of PCM. When the contact ring diameter to gap ratio ( $D \gg d$ ) is large, the ring geometry can be reduced to a standard linear-TLM model. This is done by including a correction factor to compensate for the difference between the linear and the circular ring layout. Without these correction factors the extracted  $\rho_c$  will be underestimated [57]. For practical radii (up to  $200 \mu\text{m}$ ) and gap spacing ( $4 - 48 \mu\text{m}$ ), the logarithmic term in eq. 2.17 can be evaluated using Taylor expansion and is rewritten as [56]:

$$R_{Ti} \approx \left[ \frac{R_{SH}d_i}{Z_P} + \frac{2R_{SH}l}{Z_P} \right] \times c = \left[ \frac{R_{SH}d_i}{Z_P} + 2R_C \right] \times c \quad (2.18)$$

where,  $Z_P = 2\pi(D/2)$  is the perimeter of the inner circular metal pad, and  $c$  is the correction factor:

$$c = \frac{D}{2d} \ln \left[ \frac{2L_d}{D} \right] \quad (2.19)$$

To extract the contact parameters the measured  $R_T$  values are converted to its equivalent linear model by application of this correction factor. Then  $l$  and  $R_{SH}$  values are extracted graphically by plotting the corrected measured resistance values with  $d$ . From  $l$  the  $\rho_c$  is extracted using eq. 2.12.

### Scott TLM

Scott-TLM test structures consist of a reference structure and structures with metal segments of varying length underneath the PCM layer. The reference structure consists of a PCM line without any metal segment. The top view SEM image

of the reference structure (REF) and the Scott structures (S1-S7) are shown in Fig. 2.9. Metal segments of equal length are repeatedly placed at equidistance between these two contacts such that: 1) the total length of PCM in all the structures is the same as in the reference structure and 2) the total lengths of PCM segments and the metal segments are the same. Two large metal to PCM contacts at the ends of the PCM line serve as the entry and exit contacts for the current. The number and width of the metal segments for each structure we used is given

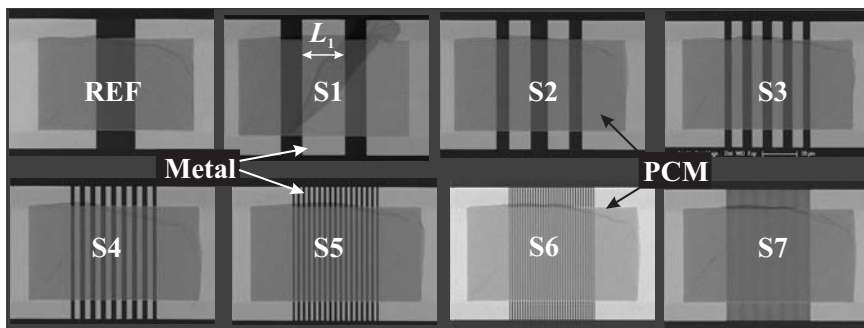


Figure 2.9: Top view SEM image of reference structure (REF) and other Scott structures (S1-S7) showing the metal segments and PCM line.

in Table 2.1. A cross-sectional schematic of the Scott structure showing the PCM layer on top of the metal segment is shown in Fig. 5.9.

Table 2.1: Metal dimensions for different Scott-TLM structures

Structure	Number ( $n$ )	Length $L_i$ ( $\mu\text{m}$ )
REF	0	0
S1	1	25
S2	2	12.5
S3	4	6.25
S4	8	3.15
S5	16	1.57
S6	32	0.78
S7	64	0.39

The measurement technique for these structures is by eliminating the resistance of the reference structure (REF) not interrupted by metal segments from the resistance of the structures (S1-S7) interrupted by one or more metal segments. As the structures have been designed to have equal PCM and electrode segments lengths, the difference between the reference resistance and the others

resistances is attributed to the total contact resistance,  $R_{CT}$ . With the metal resistance negligible compared to the sheet resistance of the PCM layer  $R_{SH}$ ;

$$R_{CT} = R_{Ti} - R_{ref} \quad (2.20)$$

where  $R_{Ti}$  is the resistance of the structure interrupted by  $n$  metal segments,  $R_{ref}$  is the resistance of the reference structure. From  $R_{CT}$ , the contribution of the contact resistance ( $R_C$ ) of the individual metal segments in a structure is expressed as:

$$R_C = \frac{R_{Ti} - R_{ref}}{n} \quad (2.21)$$

The change in  $R_C$  with the length of the metal segment  $L_i$  is shown in Fig. 2.10. With the knowledge of  $R_{SH}$  and width of the PCM segment  $W$ ,  $\rho_c$  is then extracted from  $R_C$  by fitting the measurements with the equation [55]:

$$R_C = \frac{2\sqrt{\rho_c R_{SH}} \tanh(L_i/2l)}{W} \quad (2.22)$$

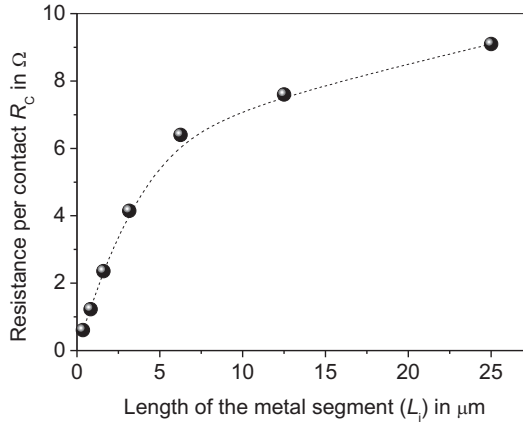


Figure 2.10: Change in  $R_C$  with length of the metal segments in the Scott structure.

When a current is forced through these Scott structures the current divides itself between the PCM layer and the metal segments, based on  $L_i$  of the structure compared to  $l$ . The two limiting cases for these structures are:

1.  $L_i \ll l$ ; the current does not have enough length to enter the metal and hence the presence of metal has little or no effect on the measured resistance.
2.  $L_i \gg l$ ; the current has enough length to completely enter the metal from the PCM, and flows through the metal before it goes back to the PCM.

In this case the metal segment shorts that part of the PCM resistance. At the same time it adds two metal to PCM contact resistances  $R_C$  and the metal segment resistance. Applying this to eq. 2.22, the limiting case of this resistance can be expressed as;

$$R_C \lim_{L_i > l} = R_0 = \frac{2\sqrt{\rho_c R_{SH}}}{W} \quad (2.23)$$

These two conditions can be understood by considering the fraction of the current  $I$  in the metal segment  $L_i$  as a function of the position  $x$ . With negligible metal resistance this is represented as [51]:

$$\frac{I(x)}{I} = \frac{\sinh(L_i/l) - \sinh(x/l) - \sinh((L_i/l) - x)}{\sinh(L_i/l)} \quad (2.24)$$

Since Scott structures are available with different metal lengths, the limiting condition for  $R_C$  in eq. 2.23 can be applied to eq. 2.22 and can be expressed as [55]:

$$\frac{R_0 + R_C}{R_0 - R_C} = \exp\left(\frac{L_i}{l}\right) \quad (2.25)$$

From the slope of the plot of eq. 2.25 as a function of  $L_i$ , the contact transfer length  $l$  is calculated and  $\rho_c$  can be extracted.

## 2.4 High frequency measurement structures

The test structures discussed so far are designed for contact resistance measurements at DC current and voltages. An embedded phase change memory cell will be accessed in a nano-second (ns) time scale during the operation of the device. They will be typically operated in the MHz frequency range. Hence the current and voltage at the contacts in this memory cell will not be static during operation. In this section a modified TLM test structure is presented which is proved to be suitable for High Frequency (HF) contact resistance measurements [59].

To be able to perform high frequency S-parameter measurements, test structures are designed in a Ground-Signal-Ground (GSG) configuration. Scott-TLM structures can be adapted in this GSG configuration. Identical test structures were fabricated on the same dies in the GSG and in the DC four terminal configurations to validate this HF approach. An SEM image of a Scott TLM structure with four metal segments in the GSG configuration and the DC configuration is shown in Fig. 2.11. From the measured S-parameters the real and the imaginary part of the differential impedance ( $Z$ ) offered by each of the structures is calculated as [60]:

$$Z = Z_{\text{diff}} = Z_{11} - Z_{21} - Z_{12} + Z_{22} \quad (2.26)$$

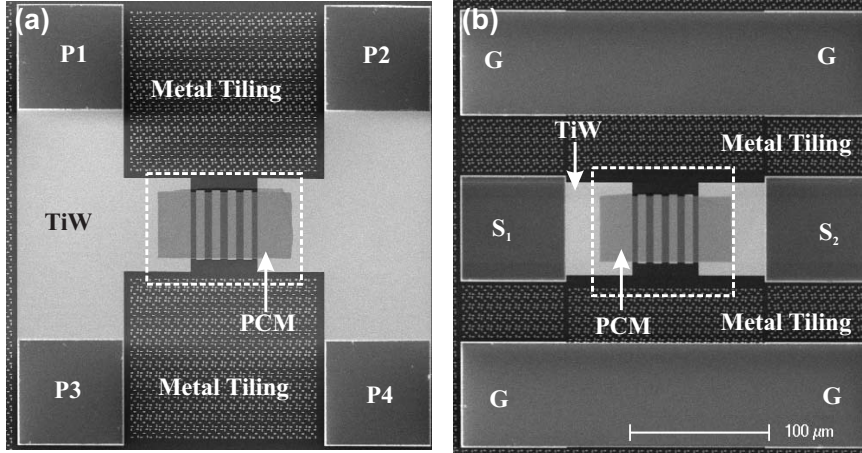


Figure 2.11: SEM image of Scott-TLM structure with the PCM line intercepted by four TiW metal segments. (a) In the GSG configuration for HF measurements. (b) In the four bond-pad configuration for DC measurements.

From this measured  $Z_{\text{diff}}$ ,  $\rho_c$  is extracted with frequency. The design rules for the HF measurement structure, fabrication details, contact resistance measurements and data extraction are presented in Chapter. 5.

## 2.5 Comparison of the test structures

Both the Kelvin and TLM methods are suitable for accurate characterization of *rectifying* and *ohmic* contacts [57]. Since the underlying principles in the parameter extraction from these structures are different these structures are subject to different geometrical design criteria and measurement limits.

A Kelvin resistor structure employs a four terminal measurement and hence measures only one contact from which  $\rho_c$  can be extracted. The value of RC determined by this method is made up of several contributions, which bear direct relevance to the contact resistances in real device contacts [61]. The determination of  $\rho_c$  is based in the assumption of having a uniform contact interfacial layer. For non uniform layers  $\rho_c$  cannot be defined since it is not constant from point to point in the contact [62]. This is presented experimentally in detail in Chapter 6.2. A design criterion for Kelvin structures is that, for accurate  $\rho_c$  extraction the size of the contact area should be such that it is completely used for current transfer (less than  $5l$ ). Another source of error in CBKR structures is when they are designed with a relatively large overlap region compared to the contact area. This leads to a larger geometrical resistance and inaccurate estimation of  $\rho_c$  [63].

In the case of TLM structures, contact resistance determination deals with



difference values rather than absolute values. TLM structures are less sensitive to overlap region since these structures are based on the transfer length principle. It detects only the front contact potential [64]. Hence the design criterion for these structures is that contact length  $L$  should be greater than  $5l$ . With  $L \gg l$ , the current density at the contact is influenced only by the contact width  $W$  and not  $L$ . An advantage of TLM structures over Kelvin structures is that these structures can be adapted in the GSG configuration suitable for HF contact resistance measurements. Limitation of a linear-TLM and circular-TLM structures:

- The main limitation of TLM structure is that it is a differential measurement and the PCM resistance is measured along with the contact resistance. This limits the accuracy of data extraction to the errors in determining the geometrical values of  $d$ ,  $W$  and  $L$ .
- If the metal resistance is not negligible compared to  $R_{SH}$ , this results in an appreciable voltage drop within the contact metal layer [58]. This situation occurs for highly resistive or thin contact metal layers. In this case the metal no longer acts as an equi-potential layer and hence in this case the transfer length approximation and model is not valid.
- The transmission line approximation also fails in the case when sheet resistance of the PCM at the contacts is different from the sheet resistance of PCM between the contacts [53][21].

The main advantage of a circular-TLM structure is that due to the circular geometry of this structure current can only flow from the central contact to the surrounding contact. Any isolation is not required. In the case of linear-TLM structures a parasitic current could flow from contact to contact in non-isolated regions [44]. Circular-TLM structures can be fabricated on blanket films using a relatively simple metal lift off process. They can be processed at a lower thermal budget [56][65].

In the case of a Scott TLM structures, most of the limitations of a linear-TLM are subdued. Sheet resistance of PCM at the contact and on the metal segments can be different from that between metal segments. In the case of high resistive metal, or thin metallic layers this resistance should be taken into account in the analytical model [50][51]. In these structures the width of the metal contact segment  $L_i$  need not be greater than the  $l$ . The limit of  $\rho_c$  that can be extracted depends directly on  $L_i$  relative to  $l$ . For commonly used lithography techniques these structures are suitable to measure metal to PCM contacts with  $\rho_c$  in the  $10^{-9} \Omega \cdot \text{cm}^2$  range, which was not possible from other TLM structures.

## 2.6 Van der Pauw structures

The knowledge of the sheet resistance  $R_{SH}$  of a PCM layer is important for  $\rho_c$  extraction from CBKR test structures and for TLM structures. In addition the

state of the PCM and its properties can also be identified from sheet resistance values. Van der Pauw structures of the type shown in Fig. 2.12 can be used for sheet resistance measurements of a thin film layer.

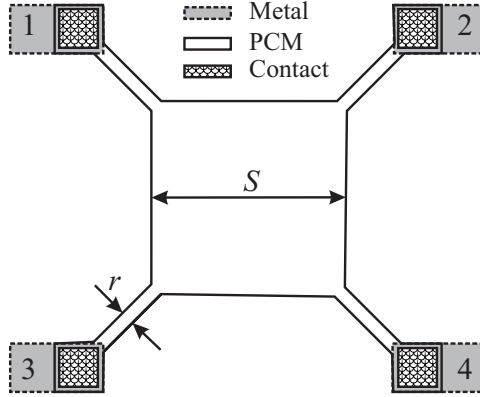


Figure 2.12: Schematic layout of a square Van der Pauw structure of side  $S$ .

To measure the sheet resistance of the layer, a current is forced from pad 1 to 2 and a voltage is measured at pad 3 and 4 in the structure. From this the resistance ( $R_V$ ) of the layer is calculated. The length of the electrical contact ( $r$ ) should be negligibly small compared to edge length of the structure ( $S$ ). An advantage of this structure is that  $R_V$  is independent of  $S$ . From  $R_V$  the sheet resistance ( $R_{SH}$ ) of the layer is obtained by using the geometrical factor, which is  $\pi/\ln(2)$  for a square structure [66][44]:

$$R_{SH} = \frac{\pi}{\ln(2)} \times \frac{V}{I} \approx 4.53 \times \frac{V}{I} \quad (2.27)$$

$R_{SH}$  is related to the Intrinsic layer resistivity ( $\rho$ ) normalized with the thickness ( $h$ ) as given by:

$$\rho = R_{SH} \times h \quad (2.28)$$

The measurement structures for  $\rho_c$  determination are always accompanied by Van der Pauw structures to accurately measure the  $R_{SH}$  values.

## Phase change material properties

*In this chapter, the relevant electrical and optical properties of two different classes of PCM are summarized. In the first part of this chapter, the temperature dependence of the resistivity of amorphous PCM is studied. From these measurements the amorphous to crystalline phase transition (crystallization) temperature, activation energy for conduction in the amorphous state and the temperature coefficient of resistance (TCR) in the crystalline state are determined. In the following section, the optical band gap and absorption coefficient for doped-Sb<sub>2</sub>Te is determined from ellipsometric measurements. In the last part of this chapter, the carrier type, the concentration and the mobility in the crystalline PCM is determined from Hall effect measurements. The knowledge of these parameters is essential for understanding and modelling the electrical charge transport mechanism at the metal to PCM interfaces.*

### 3.1 Phase change resistivity measurements

In the application of PCM as embedded RAM, the electrical properties are of importance for write, erase and read operation. Phase change materials can be divided into two classes based on their crystallization mechanisms; nucleation dominated and growth dominated materials [67][8]. Phase change materials with composition on the tie-line  $\text{GeTe-Sb}_2\text{Te}_3$  in the phase diagram are classified as nucleation dominated materials. If these materials are sufficiently heated in the amorphous state crystallites nucleate in the layer, followed by growth of these nuclei over a small distance until they impinge on other crystallites [9]. These materials have a large nucleation probability, which occurs rather fast. Materials with a composition around the eutectic point  $\text{Sb}_{69}\text{Te}_{31}$  are growth dominated [8]. These materials have a lower nucleation probability, but once a crystallite is formed it grows faster. In the application for optical data storage, the crystallization initiates from the amorphous to crystalline interface, i.e. there is no nucleation needed [8]. In the application for memories; the Ovonic Unified Memory (OUM) cell uses a nucleation dominated material, in particular the composition  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  is known to yield good results, for memory line cells a growth dominated doped- $\text{Sb}_2\text{Te}$  material is preferred, doped with one or more elements from the series Ge, In, Ag and Ga [5].

The change in resistivity of an amorphous thin film of doped- $\text{Sb}_2\text{Te}$  and  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  with temperature is shown in Fig. 3.1. These measurements were performed on Van der Pauw structures in a  $\text{N}_2$  atmosphere with a temperature ramp rate of  $5\text{ }^\circ\text{C}/\text{min}$ .

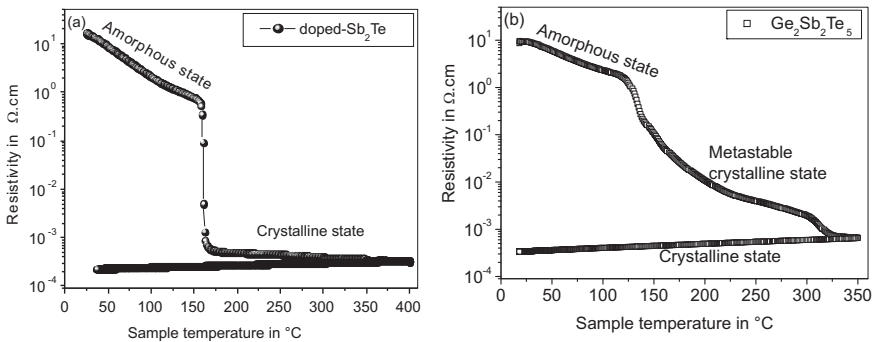


Figure 3.1: Change in resistivity of amorphous (a) doped- $\text{Sb}_2\text{Te}$  and (b)  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  with thermal cycle.

At crystallization, at approximately  $150\text{ }^\circ\text{C}$ , the resistivity of the layer decreases by more than three orders of magnitude. The temperature at which this transition occurs is called crystallization temperature. The crystallization temperature as such depends on the type of the phase change material, the temperature ramp rate, the surrounding layers and other parameters [8]. A ramp

rate of 5 °C/min for uncapped thin films of 20 nm, the crystallization temperature of doped-Sb<sub>2</sub>Te is 154 °C and for Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> is approximately 130 °C [5]. Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> is observed to have a phase transformation in the crystalline state at a higher temperature of approximately 300 °C; it changes from the meta-stable fcc phase into the stable hexagonal phase [68]. This large contrast in resistivity between the amorphous and the crystalline state is employed to realize a PCRAM cell [5].

In the amorphous state, the resistivity/conductivity of the PCM follows an Arrhenius type exponential relation with temperature. This is expressed as [69]:

$$\sigma = \sigma_0 \exp\left(\frac{-E_A}{k_b T}\right) \quad (3.1)$$

From eq. 3.1,  $E_A$  can be calculated. The change in conductivity ( $\sigma$ ) of amorphous PCM layer with temperature in the range from -40 °C to 60 °C is shown in Fig. 3.2.

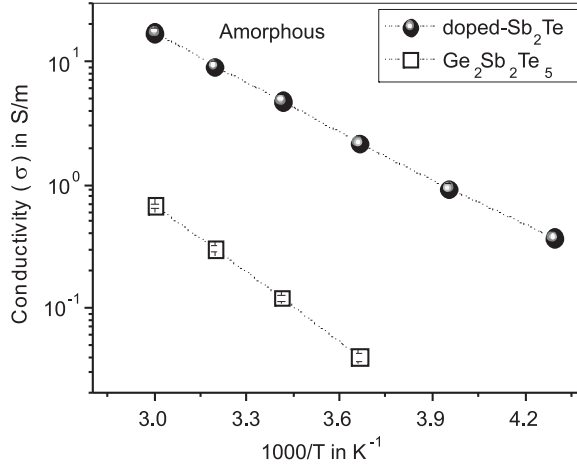


Figure 3.2: Change in  $\sigma$  with temperature measured for amorphous PCM layers.

In the amorphous state, an  $E_A$  for conductivity of 0.26 eV is calculated for doped-Sb<sub>2</sub>Te and 0.35 eV for Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub>. For uncapped PCM layers, with a thickness in the range of 5 to 200 nm, the same crystallization temperature and  $E_A$  is observed. In the crystalline state PCM shows metallic characteristics. A linear dependence of resistivity ( $\rho$ ) with temperature is observed as shown in Fig. 3.3(a). The calculated TCR of crystalline PCM after anneal at a temperature in the range 150 to 400 °C is shown in Fig. 3.3(b). In the crystalline state low TCR is observed for both PCM's. After anneal at a higher temperature the sign of the TCR changes. This transition depends on the annealing time and temperature. In the perfect crystalline state, a positive TCR is observed.

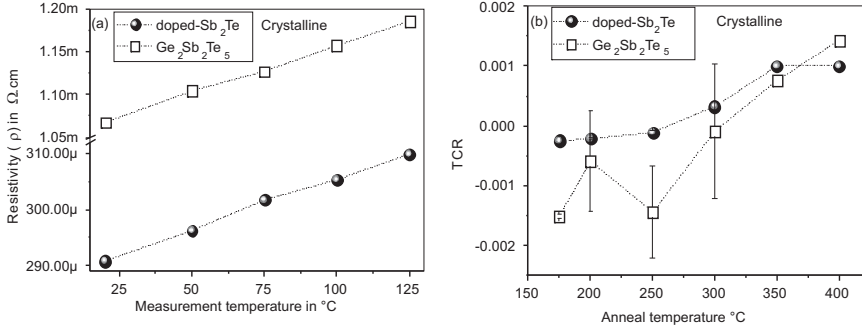


Figure 3.3: Change in  $\rho$  with temperature for crystalline PCM layers ( $\rho$  scale has a break in between) (b) the calculated TCR for crystalline PCM after anneal at temperatures in the range 150 to 400  $^{\circ}\text{C}$ .

## 3.2 Optical properties of phase change materials (PCM)

The first commercial application of PCM for data storage is in CD and DVD rewritable. Write, erase and readout of data are done optically. For light of a specific wavelength ( $\lambda$ ) the optical constants are expressed as the complex refractive index, expressed as  $n + jk$ , where  $n$  is the reflective index and  $k$  is the extinction coefficient. These optical constants of the material are determined from optical transmission and reflection ellipsometric measurements. The change in  $n$  and  $k$  values with photon energy,  $E_P$  for doped-Sb<sub>2</sub>Te in the amorphous state is shown in Fig. 3.4. The reported  $n$  and  $k$  values for similar PCM exhibits identical

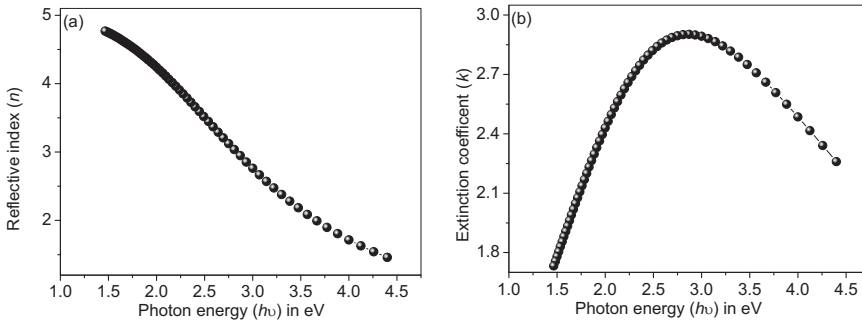


Figure 3.4: Change in the  $n$  and  $k$  value with photon energy for doped-Sb<sub>2</sub>Te in the amorphous state.

behavior in this wavelength range [70][71][8].

If a light beam with intensity  $I_0$  propagates over a distance  $x$  in the material,

then the intensity decreases to  $I$ , which can be expressed as [44]:

$$I = I_0 \exp(-\alpha x) \quad (3.2)$$

where,  $\alpha$  is the absorption coefficient of the material. With the knowledge of the optical constants, the absorption coefficient  $\alpha$  of a material can be calculated.  $\alpha$  is related to  $k$  as:

$$\alpha = \frac{4\pi k}{\lambda} \quad (3.3)$$

These optical properties of the PCM play an important role in the experimental section in Chapter 4.

The optical band gap,  $E_g^{\text{opt}}$  of a material is determined by the onset of optical absorption that occurs when the photon energy of the incident light just equals the energy separation of the highest occupied electron states in the valence band and the lowest empty states in the conduction band. Photons with energy greater than this energy separation are absorbed. Light with energy less than the band-gap will be transmitted or reflected. Hence  $E_g^{\text{opt}}$  is determined by measuring  $\alpha$  with  $E_P$ , which is related as [8]:

$$\alpha h\nu = (\text{constant})(h\nu - E_g^{\text{opt}})^r \quad (3.4)$$

In the case of indirect band-gap materials  $r = 2$  (*Tauc* plot), or for direct gap materials  $r = 1/2$ . The plot of  $(\alpha h\nu)^{1/2}$  with  $E_P$  and  $(\alpha h\nu)^2$  with  $E_P$  for doped-Sb<sub>2</sub>Te in the amorphous state is as illustrated in Fig. 3.5(a) and Fig. 3.5(b) respectively.

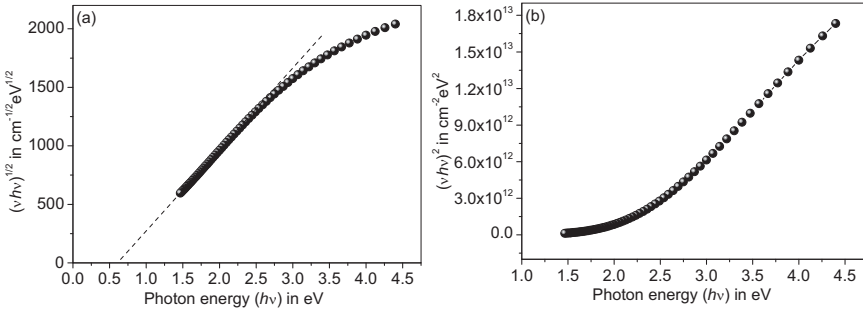


Figure 3.5: (a) Plot of  $(\alpha h\nu)^{1/2}$  with  $E_P$  for amorphous doped-Sb<sub>2</sub>Te. of 0.6 eV is calculated from this plot. (b) Plot of  $(\alpha h\nu)^2$  with  $E_P$

The relation with  $r$  of 2 is valid for chalcogenide materials indicating that these are indirect band-gap materials [72]. The calculated for doped-Sb<sub>2</sub>Te in the amorphous state is 0.6 eV. Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> is reported to be an indirect gap material with a of 0.7 eV in the amorphous state and 0.5 eV in the crystalline state [8][73].

### 3.3 Hall effect measurements on PCM

In this section the carrier concentration  $N_C$ , mobility  $\mu$ , and polarity of the charge carrier ( $n$ -type or  $p$ -type) of crystalline PCM are determined from Hall effect measurements. The Hall effect [74] arises due to the existence of Lorentz force, which is the combination of electric force and magnetic force. When the charge carriers involved in the conduction, move along an electric field  $\vec{E}$  with a speed  $\vec{v}$  and with a direction perpendicular to an applied magnetic field  $\vec{B}$ , they experience a magnetic force ( $q\vec{v} \times \vec{B}$ ) acting normal to both directions. This is schematically represented in Fig. 3.6.

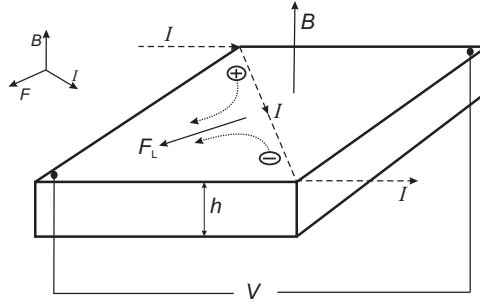


Figure 3.6: Schematic illustration of a Hall bar, showing the direction of  $B$ ,  $I$  and the resulting  $F_L$ .

The resulting Lorentz force  $\vec{F}_L$ , on the charge carriers due to the electromagnetic field is given by the vector representation [31][44]:

$$\vec{F}_L = q(\vec{E} + \vec{v} \times \vec{B}) \quad (3.5)$$

This internal force deflects the charge carriers generating an electric field within the layer. The polarity/direction of this field is determined by the nature of the majority charge carrier involved in conduction. Given the direction of magnetic field  $B$  and a positive current  $I$  as illustrated in Fig. 3.6, positive charge carriers are deflected to the left side (direction of  $\vec{F}_L$ ). This results in a more positive potential at this half compared to the right half. The induced Hall field will be diagonally from the left corner to the right corner. In the case of electrons, the potential at the left side becomes more negative due to localization of electrons. This results in an opposite Hall field. Assuming an energy independent scattering mechanism, the induced Hall field, expressed as the Hall voltage,  $V_H$ , is [44]:

$$V_H = \frac{BI}{qhN_C} \quad (3.6)$$

where  $h$  is the thickness of the layer,  $q$  is the elementary charge and  $N_C$  is the



carrier concentration. From this, the Hall coefficient  $R_H$  is derived as:

$$R_H = \frac{HV_H}{BI} \quad (3.7)$$

The charge carrier density in the layer is then expressed as:

$$N_C = \frac{1}{qR_H} \quad (3.8)$$

Assuming that only one type of carriers involved in the conduction, the electrical conductivity  $\sigma$  of the layer, is related to the electrical mobility  $\mu$  of the charge carriers in the layer by:

$$\sigma = q\mu N_C \quad (3.9)$$

Hall effect measurements were performed on Van der Pauw structures, used for sheet resistance measurements [66]. The electrical connections of a square Van der Pauw structure for sheet resistance measurements and for Hall effect measurements are shown in Fig. 3.7.

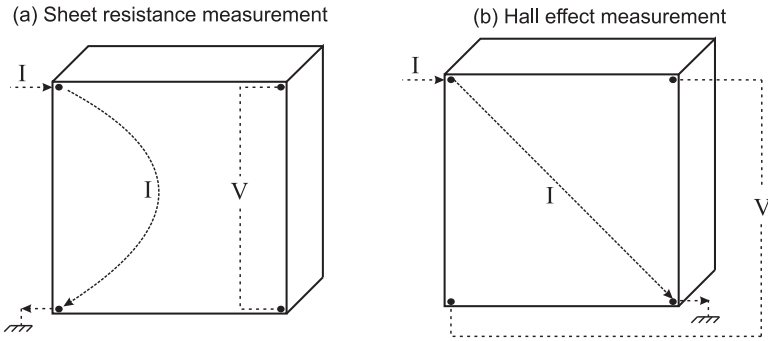


Figure 3.7: Schematic of a square Van der Pauw structure in the sheet resistance measurement and Hall effect measurement configuration.

To perform Hall measurements, a current  $I$  is forced through the layer and the resulting voltage,  $V$  is monitored with and without magnetic field. To check the symmetry, these measurements were performed with positive and negative currents and with magnetic field in opposite directions. The measured  $I$ - $V$  characteristics with different  $B$  for crystalline doped-Sb<sub>2</sub>Te are shown in Fig. 3.8(a).

The measured voltage is symmetrical and it increases with  $I$  and  $B$ . Fig. 3.8(b) shows the measurements on doped-Sb<sub>2</sub>Te; without magnetic field and with a magnetic field of 1 Tesla only (applied in opposite directions). The difference in voltage measured with and without magnetic field is the Hall voltage ( $V_H$ ). For a fixed positive  $I$  through the layer,  $V$  increases with the application of a positive  $B$ . This implies that the charge carriers in doped-Sb<sub>2</sub>Te in the crystalline

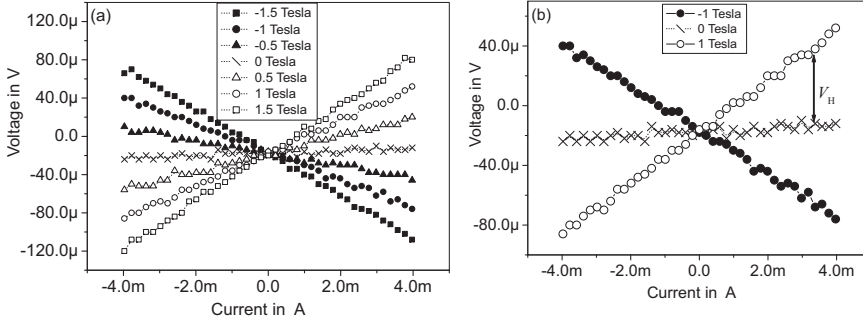


Figure 3.8: Change in measured voltage with  $I$  and  $B$  for crystalline doped-Sb<sub>2</sub>Te.

state are positively charged. Similar measurements performed on doped-Sb<sub>2</sub>Te and Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> samples annealed at different temperatures in the range from 250 °C to 400 °C also show  $p$ -type conduction. From these measurements  $V_H$ ,  $N_C$  and  $\mu$  are calculated using eq. 3.6 to eq. 3.9. These calculated  $N_C$  and  $\mu$  values for both crystalline PCM materials are shown in Fig. 3.9. The  $N_C$  values for doped-

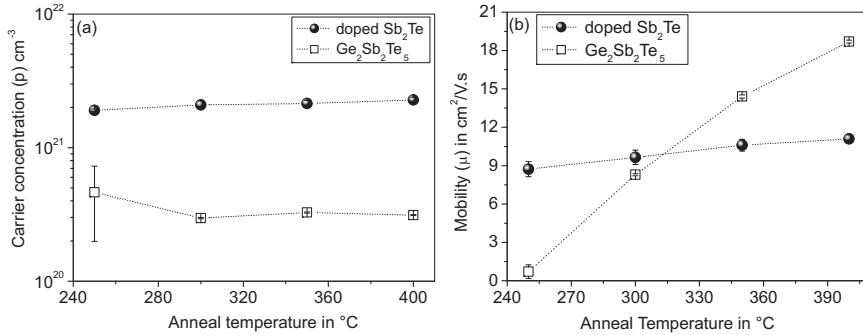


Figure 3.9: Change in  $N_C$  and  $\mu$  with anneal temperature.

Sb<sub>2</sub>Te and Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> remain constant upon annealing up to 400 °C. The  $N_C$  for doped-Sb<sub>2</sub>Te is approximately  $2 \times 10^{21}$  cm<sup>-3</sup>. This is one order of magnitude higher than that of Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> ( $\approx 5 \times 10^{20}$  cm<sup>-3</sup>). Our measured values for Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> agree well with the reported values [8][73]. The calculated  $\mu$  increases upon annealing at higher temperatures, as shown in Fig. 3.9(b). This increase in  $\mu$  is more pronounced for Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub>. The value of  $\mu$  and  $N_C$  are related to the resistivity by eq. 3.9. Hence the observed decrease in resistivity upon annealing is due to the increase in the mobility of the charge carriers rather than a higher  $N_C$  [75]. In this case during heating crystallites grow and the scattering of the charge carriers at the grain boundaries decreases [68]. This results in an increased mobility [8].

Fig. 3.10 shows the change in the  $N_C$  and  $\mu$  with measurement temperature for crystalline doped-Sb<sub>2</sub>Te and Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub>.  $N_C$  hardly changes with temperature, but  $\mu$  decreases slightly with temperature.

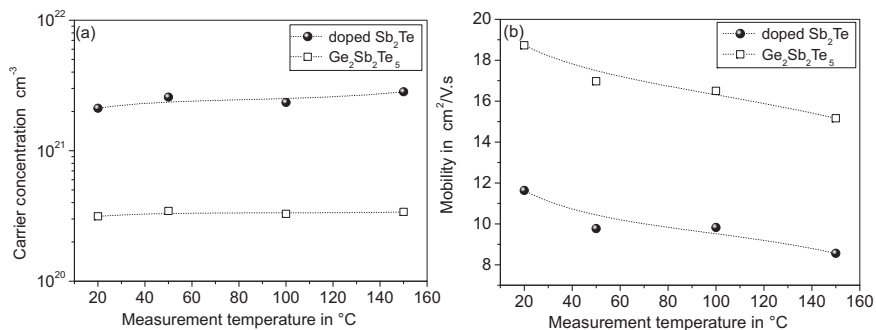


Figure 3.10: Change in  $N_C$  and  $\mu$  with measurement temperature.

Measurements on high resistive samples in the amorphous state of the PCM show large experimental errors. This limits measurements on crystalline PCM only. In addition, use of higher magnetic field can mitigate this problem. Finally, to confirm the measurement results and to calibrate the Hall effect measurement setup, *p*-type and *n*-type silicon samples with a known  $N_C$  were fabricated and measured. The details are given in Appendix A3.1.

### 3.4 Summary

The electrical properties of growth dominated doped Sb<sub>2</sub>Te and nucleation dominated Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> were investigated. When heated at a ramp rate of 5 °C/minute amorphous doped-Sb<sub>2</sub>Te crystallizes at 150 °C and Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> at around 130 °C. In the amorphous state both the PCM's exhibit an exponential dependence with temperature with an activation energy of 0.26 eV for doped-Sb<sub>2</sub>Te and 0.35 eV for Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub>. The calculated optical band gap for doped-Sb<sub>2</sub>Te from ellipsometric measurements is 0.6 eV. In the crystalline state, an almost zero TCR is observed for both the PCM with *p*-type conduction. The calculated carrier density from Hall effect measurements is 2 × 10<sup>21</sup> cm<sup>-3</sup> for doped-Sb<sub>2</sub>Te and 5 × 10<sup>21</sup> cm<sup>-3</sup> for Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub>. When annealed at a higher temperature, in the crystalline state the carrier concentration remains constant while the mobility increases.



## Electrical characteristics of electrode to PCM contacts

The aim of this chapter is to provide the reader with a complete understanding of contacts for metal to PCM in the amorphous and in the crystalline states. The first step in the understanding of these contacts is to accurately determine the electrical contact resistance. Dedicated test structures were fabricated from which the contact resistance is electrically determined. This measured value is expressed in terms of specific contact resistance  $\rho_c$ , which is a suitable parameter to compare different contacts. The next level of understanding of these contacts is to physically model the charge transport mechanism, based on the measured values.

In the first section of this chapter,  $\rho_c$  is extracted and compared for identical metal to PCM contacts using the Kelvin resistor method and the transfer length method. This is performed for both the amorphous and crystalline state of two classes of PCM. The temperature and voltage bias dependence of  $\rho_c$  for these contacts are also studied. In the second section, the  $\rho_c$  is extracted for doped-Sb<sub>2</sub>Te to different CMOS compatible electrodes W, TiW, Ta, TaN and TiN. Based on these measurements, the barrier formation and charge transport mechanism at the contact is modeled. Reset current reduction for maximum power transfer is an essential requirement for the scaling of PCRAM cells. In these devices this can be influenced by changing layer thickness of the PCM. In the following section the change in contact resistance with the layer thickness is studied. Measurements on structures with ultra thin PCM layers under different illumination conditions indicated the existence of a modified region in the PCM at the interface. A detailed understanding of these contacts is essential for selection of the electrode metal for design, integration, scaling, modeling and optimization of PCRAM cells.

## 4.1 Comparison of TiW to PCM contact resistance measurements

Determination of the metal to PCM contact resistance is the first step towards understanding of the contacts in a PCRAM cell. With the knowledge of the  $\rho_c$  values, the contacts in the memory cell can be optimized for maximum power transfer during switching. In this section, the contact resistance between titanium tungsten ( $\text{Ti}_{0.3}\text{W}_{0.7}$ ) electrodes to two classes of phase change materials, growth-dominated doped- $\text{Sb}_2\text{Te}$  and nucleation-dominated  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  is experimentally characterized. The  $\rho_c$  values are systematically determined for the PCM in the amorphous and crystalline states. To be able to measure the contact resistance to amorphous PCM the test structures should be processed below the crystallization temperature of PCM. The amorphous to crystalline transition temperature for doped- $\text{Sb}_2\text{Te}$  is 160 °C and for  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  crystallization starts at 130 °C [5]. Hence the test structures (Kelvin resistor and TLM) were fabricated with a maximum thermal budget of 120 °C. The extracted  $\rho_c$  from Kelvin resistor method and TLM structures is compared for identical contact materials. Measurement details and data extraction procedure from these test structures are described in Chapter 2.3. In the last part of this section, the charge transport mechanism at the metal to PCM interface is modeled based on the temperature and voltage bias dependence of  $\rho_c$ .

### 4.1.1 Kelvin resistor measurements

Cross Bridge Kelvin Resistor (CBKR) structures are suitable for direct measurement of interfacial contact resistance. The top view SEM image and the schematic cross-section of this test structure used for the measurements is shown in Fig. 2.3. To fabricate these structures, 50 nm TiW is deposited on an oxidized silicon wafer and patterned to form the bottom electrode layer of the contact. The top layer is 20 nm PCM which is deposited amorphous by sputtering. The contact area  $A$  between the two layers is defined by a contact hole formed in a 40 nm PECVD  $\text{SiO}_2$  layer. These structures are fabricated with a metal to PCM contact area ranging from 1  $\mu\text{m}^2$  to 16  $\mu\text{m}^2$  with different overlap lengths ( $\delta$ ) ranging from 0.2  $\mu\text{m}$  to 5  $\mu\text{m}$ . The exact dimensions of the  $A$  and the  $\delta$  are determined using an SEM. Resistance measurements were performed on these fabricated structures after annealing at different temperatures for 5 min in an  $\text{N}_2$  atmosphere. Annealing the structures at temperatures above the crystallization temperature transforms the PCM in these structures to the crystalline state. Structures annealed above 250 °C were protected against oxidation and evaporation by capping with a 50 nm PECVD  $\text{SiO}_2$  layer deposited at 250 °C.

The change in measured resistance,  $R_K$  with  $\delta$  for TiW to doped- $\text{Sb}_2\text{Te}$  CBKR structures with  $A$  of 4  $\mu\text{m}^2$  is shown in Fig. 4.1. These measurements are shown for the amorphous (a) and the crystalline (b) state of doped- $\text{Sb}_2\text{Te}$ . The  $\rho_c$  is

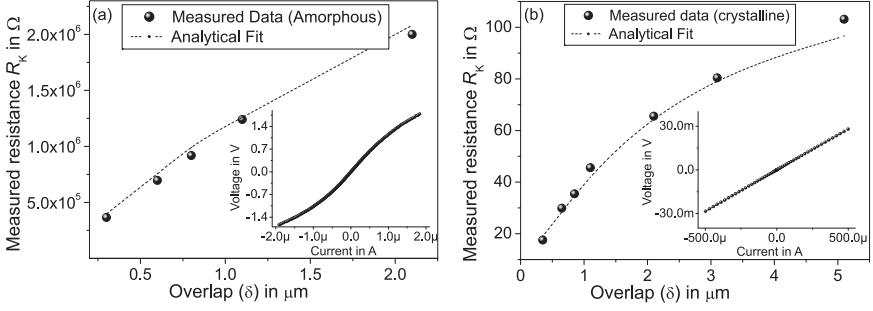


Figure 4.1: Change in  $R_K$  with  $\delta$  for CBKR structures with  $A$  of  $4 \mu\text{m}^2$  (a) PCM in the amorphous state and (b) in the crystalline state.  $\bullet$  represent the measured points and the line represents the fit based on the 2D model. The inset figure shows the typical  $I$ - $V$  curve for a measurement point.

extracted from  $R_K$  excluding the resistance in the  $\delta$  region using the 2D analytical model as represented by eq. 2.10. The fit for  $R_K$  values based on the extracted  $\rho_c$  is derived using eq. 2.10, and the sheet resistance  $R_{SH}$  of the PCM measured on Van der Pauw structures on the same die. The measured  $R_K$  and the derived fit show good agreement.  $R_K$  measurements and  $\rho_c$  extraction were performed for different contact areas on different dies on the wafer. The average extracted  $\rho_c$  values for TiW to doped-Sb<sub>2</sub>Te and TiW to Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> in the amorphous and crystalline state, when annealed at different temperatures up to 400 °C, is shown in Fig. 4.2. The error bar indicates the spread in the extracted values at each point. A summary of the extracted  $\rho_c$  for amorphous and crystalline PCM (after 175 °C anneal and 400 °C anneal) is given in Table 4.1. The resistivity ( $\rho$ ) of the PCM measured on Van der Pauw structures is also given.

Table 4.1: TiW to PCM  $\rho_c$  (in  $\Omega.\text{cm}^2$ ) and corresponding PCM resistivity  $\rho$  (in  $\Omega.\text{cm}$ ) with anneal temperature

Contact	120 °C anneal	175 °C anneal	350 °C anneal
doped-Sb <sub>2</sub> Te; $\rho_c$	$(4.2 \pm 0.3) \times 10^{-3}$	$(3.4 \pm 2.2) \times 10^{-7}$	$(1.2 \pm 0.4) \times 10^{-7}$
doped-Sb <sub>2</sub> Te; $\rho$	21.6	$540 \times 10^{-6}$	$250 \times 10^{-6}$
Ge <sub>2</sub> Sb <sub>2</sub> Te <sub>5</sub> ; $\rho_c$	$(9.5 \pm 0.8) \times 10^{-2}$	$(3.8 \pm 0.6) \times 10^{-6}$	$(1.9 \pm 0.7) \times 10^{-7}$
Ge <sub>2</sub> Sb <sub>2</sub> Te <sub>5</sub> ; $\rho$	805	$20 \times 10^{-3}$	$524 \times 10^{-6}$

In the amorphous state, the extracted  $\rho_c$  for Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> is 20 times higher than for doped-Sb<sub>2</sub>Te. When annealed at 130 °C and above, the  $\rho_c$  values for Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> show a gradual decrease up to 250 °C, as the PCM changes to the meta-stable crystalline state. Doped-Sb<sub>2</sub>Te when annealed at 150 °C, there is a sharp change in  $\rho_c$  values as the PCM changes from the amorphous to the

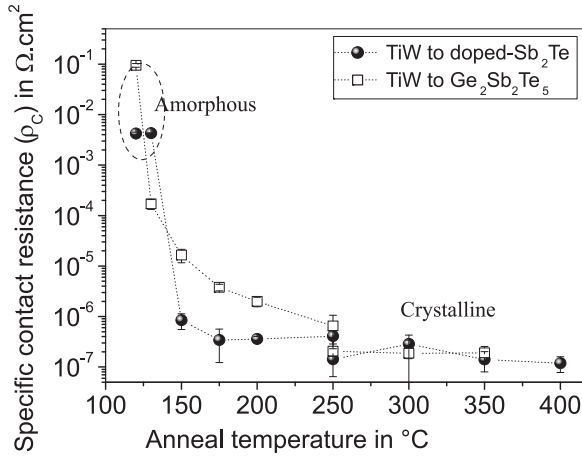


Figure 4.2: Extracted  $\rho_c$  for TiW to doped-Sb<sub>2</sub>Te and Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> from CBKR structures after 120 °C to 250 °C anneal and after 250 °C to 400 °C anneal using oxide capping layer. These measurements were performed at 20 °C.

crystalline phase. From these measurements, a  $\rho_c$  of  $1.2 \times 10^{-7} \Omega.\text{cm}^2$  is extracted for TiW to Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> after 350 °C anneal. This is in good agreement with a  $\rho_c$  value of  $2.6 \times 10^{-7} \Omega.\text{cm}^2$  reported for Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> contacts in OUM cells [17]. Annealing at the highest temperature of 350-400 °C, which is common for CMOS processing, the crystalline state is stable showing a  $\rho_c$  value of  $(1 - 2) \times 10^{-7} \Omega.\text{cm}^2$  for both the materials. These  $\rho_c$  values measured in the crystalline state of PCM are at least one order of magnitude above the minimum measurement range of approximately  $10^{-8} \Omega.\text{cm}^2$  for the CBKR structures [76].

#### 4.1.2 Transfer Length Method measurements

The TLM structure used for our measurements is the circular-TLM structure shown in Fig. 2.8. Each of these structures consists of a circular inner contact of the same diameter  $D$  and surrounding outer contact separated by a ring shaped gap spacing,  $d$  of different lengths. Circular-TLM structures are selected due to their advantages of having a circular geometry (discussed in section 2.3). These structures were fabricated with a relatively simple metal liftoff process with a low thermal budget (Details in Appendix A4). Using the metal liftoff process, test structures were fabricated and  $\rho_c$  is extracted for TiW to doped-Sb<sub>2</sub>Te and Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> in the amorphous and crystalline states.

The electrical characteristics of each circular-TLM structure is determined by current-voltage measurements performed using a semiconductor parameter analyzer. A normalized  $I$ - $V$  characteristic measured on a TiW to Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> circular-TLM structure with PCM in the amorphous state and crystalline state



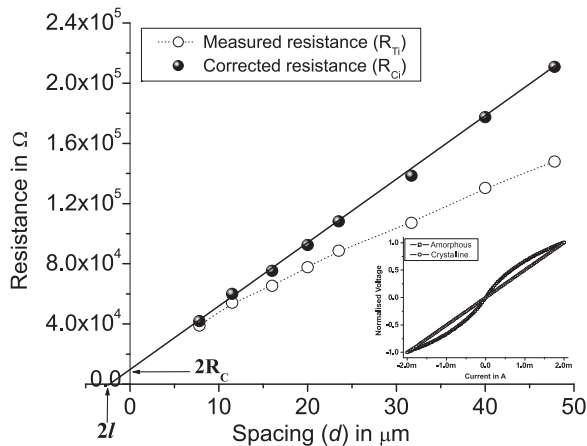


Figure 4.3: Change in measured resistance,  $R_{Ti}$  and corrected resistance,  $R_{Ci}$  with the gap spacing for circular-TLM structures. The estimation of transfer length,  $l$  from the measurements is also shown. The inset shows the normalized  $I$ - $V$  characteristics for TiW to  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  with PCM in the amorphous and crystalline state.

is shown in inset in Fig. 4.3. In the amorphous state, a nonlinear  $I$ - $V$  characteristic is observed while the crystalline state shows a linear  $I$ - $V$  characteristic. Similar characteristics are observed in the case of TiW to doped- $\text{Sb}_2\text{Te}$  contacts. The measured resistance ( $R_{Ti}$ ) of the circular-TLM structure is shown in Fig. 4.3 (open circles).  $R_{Ti}$  increases with the gap spacing (eq. 2.18). Due to the circular geometry of the gap,  $R_{Ti}$  varies non-linearly with the gap spacing. This non-linear relation is transformed into a linear curve by application of the correction factor,  $c$  in eq. 2.19 to  $R_{Ti}$ . The corrected circular-TLM resistance values,  $R_{Ci} (= R_{Ti}/c)$  varies linearly with gap spacing. The change in  $R_{Ti}$  and  $R_{Ci}$  values with the gap spacing is shown in Fig. 4.3.

From extrapolation of the line, two times the contact resistance, ( $2R_C$  at  $d = 0$ ) and two times the transfer length, ( $-2l$  at  $R_C = 0$ ) are obtained. The sheet resistance,  $R_{SH}$  of the PCM layer is calculated from the slope of the line.  $\rho_c$  is then calculated from  $l$  using the eq. 2.12. Resistance measurements and  $\rho_c$  extraction were performed on TiW to doped- $\text{Sb}_2\text{Te}$  and TiW to  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  circular-TLM structures fabricated at  $120^\circ\text{C}$ . Starting from the amorphous state, measurements were performed on the structures annealed at different temperatures up to  $250^\circ\text{C}$  (5 minutes in a  $\text{N}_2$  atmosphere). The change in extracted  $\rho_c$  is shown in Fig. 4.4.

The extracted  $\rho_c$  for TiW to doped- $\text{Sb}_2\text{Te}$  contacts decreases sharply from  $9.1 \times 10^{-3} \Omega.\text{cm}^2$  to  $6.8 \times 10^{-7} \Omega.\text{cm}^2$  when the PCM changes from the amorphous to the crystalline state. In the crystalline state,  $\rho_c$  does not change much with temperature. In the case of TiW to  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  contacts, the extracted  $\rho_c$  from

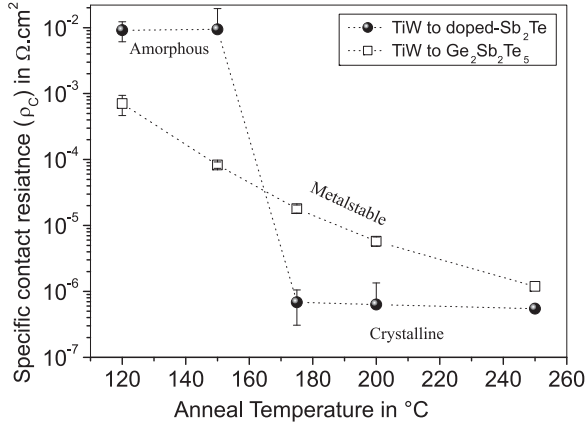


Figure 4.4: The extracted  $\rho_c$  for TiW to doped-Sb<sub>2</sub>Te and Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> from circular-TLM structures. Measurements were performed at room temperature after anneal.

these structures after fabrication is  $7 \times 10^{-4} \Omega.\text{cm}^2$ . A measured resistivity of  $6 \Omega.\text{cm}$  indicates that this PCM is in the metastable state or is partially amorphous. Upon annealing at higher temperatures,  $\rho_c$  decreases gradually as the Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> changes from the meta-stable fcc phase to hexagonal phase. A summary of the extracted  $\rho_c$  after fabrication and annealing at 175 °C and 250 °C is given in Table 4.2. The state of the PCM in these structures is confirmed by PCM resistivity values.

Table 4.2: TiW to PCM  $\rho_c$  (in  $\Omega.\text{cm}^2$ ) and corresponding PCM resistivity  $\rho$  (in  $\Omega.\text{cm}$ ) with anneal temperature

Contact	120 °C anneal	175 °C anneal	350 °C anneal
doped-Sb <sub>2</sub> Te; $\rho_c$	$(9.2 \pm 3) \times 10^{-3}$	$(6.8 \pm 6.7) \times 10^{-7}$	$(5.5 \pm 0.0) \times 10^{-7}$
doped-Sb <sub>2</sub> Te; $\rho$	16	$502 \times 10^{-6}$	$449 \times 10^{-6}$
Ge <sub>2</sub> Sb <sub>2</sub> Te <sub>5</sub> ; $\rho_c$	$(7 \pm 2) \times 10^{-4}$	$(1.8 \pm 0.2) \times 10^{-5}$	$(1.2 \pm 0.0) \times 10^{-6}$
Ge <sub>2</sub> Sb <sub>2</sub> Te <sub>5</sub> ; $\rho$	6	$23 \times 10^{-3}$	$3.9 \times 10^{-3}$

### 4.1.3 Comparison of Kelvin and TLM measurements

Contact resistance expressed in terms of  $\rho_c$  gives the magnitude of the electrical resistance encountered by the charge carriers at the metal to PCM interface. Upon crystallization, structural changes take place in the PCM alloys and subsequently change the charge transport at the metal to PCM interface. *This results in lower  $\rho_c$  values and PCM resistivity.* The  $\rho_c$  values extracted for TiW to doped-Sb<sub>2</sub>Te

and TiW to  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  from CBKR structures (Kelvin resistor method) and circular-TLM (transfer length method) structures are compared in Fig. 4.5. This data is presented for amorphous (a) and crystalline (b) PCM.

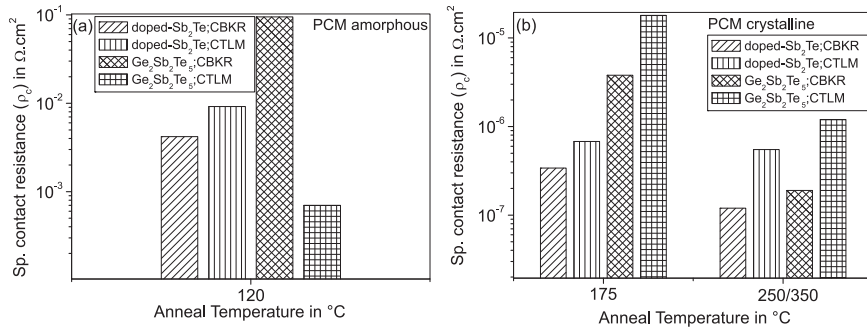


Figure 4.5: Comparison of  $\rho_c$  values extracted using Kelvin resistor method and transfer length method (CTLM) with PCM in the amorphous state (a) and crystalline state (b).

In the amorphous state of doped- $\text{Sb}_2\text{Te}_3$ , the extracted  $\rho_c$  is approximately the same for both methods. For  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ , the large difference in  $\rho_c$  is attributed to the fact that PCM is in a metastable phase in these structures. In the crystalline state, the extracted  $\rho_c$  values from both structures are in the same range. *Even though the differences are not large, the extracted  $\rho_c$  for identical TiW to PCM contacts from CBKR structures are systematically slightly lower.* This could be due to the difference in data extraction procedure from these structures. In the TLM structures  $\rho_c$  is extracted graphically, while the Kelvin method employs direct four terminal measurements of the average potential at the contact interface, and the numerical extraction of  $\rho_c$ . Further-on in this chapter, the Kelvin resistor method is employed to characterize the contact properties and to establish the charge transport at the interface.

#### 4.1.4 Temperature dependence of contact resistance

In this section, the effect of measurement temperature on measured contact resistance and extracted  $\rho_c$  is studied. The change in  $I$ - $V$  characteristic of CBKR structures when measured at different temperatures in the range from 0 °C to 60 °C for doped- $\text{Sb}_2\text{Te}_3$  and  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  in the amorphous state is shown in Fig. 4.6. These measurements were performed with a positive voltage across the contact. A positive voltage ( $V_{\text{PCM}} - V_{\text{Metal}}$  positive) implies a higher potential on the PCM side relative to the metal. For negative voltages, similar characteristics are observed with a slight asymmetry. In the crystalline state the  $I$ - $V$  characteristics hardly change with temperature.

The current through the structures increases when measured at higher temperature. The Kelvin resistance,  $R_K$  of a contact is calculated at an infinitesimal

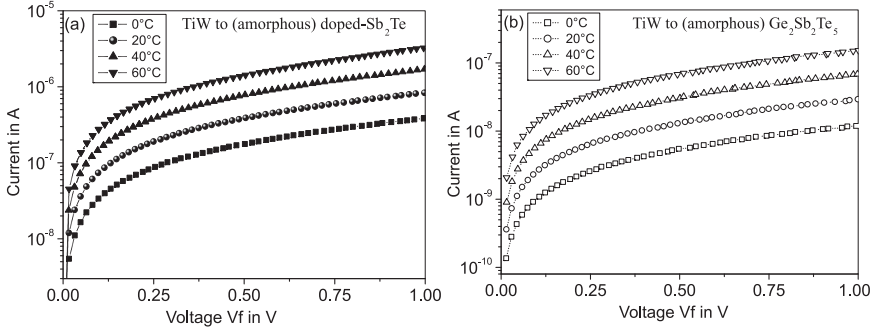


Figure 4.6: Semi-logarithmic  $I$ - $V$  characteristics measured for TiW to amorphous PCM structures.

region around zero (eq. 2.2). The change in this  $R_K$  with delta of TiW to amorphous doped-Sb<sub>2</sub>Te CBKR structures in the temperature range of -20 °C to 60 °C is shown in Fig. 4.7(a). Similar measurements with temperature (-40 °C to 100 °C) in the crystalline state of PCM is shown in Fig. 4.7(b). These measurements are for structures with a contact area of 4 μm<sup>2</sup>. As expected, the  $R_K$  values

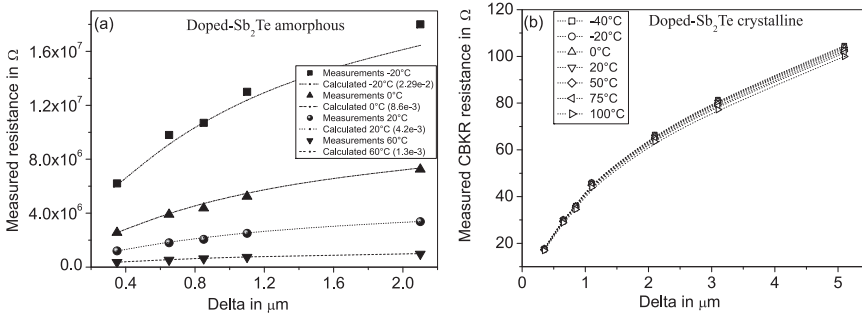


Figure 4.7: The change in measured CBKR resistance with delta for different temperatures with PCM in the (a) amorphous and (b) crystalline state.

increase with delta for all the temperatures. In the amorphous state, the  $R_K$  values show a significant change with temperature while in the crystalline state, there is not much variation.  $\rho_c$  values are extracted from these measurements for each temperature using eq. 2.10. The change in extracted  $\rho_c$  with measurement temperature for both PCM's in the amorphous and crystalline state are shown in Fig. 4.8. In the amorphous state (Fig. 4.8(a)),  $\rho_c$  shows a strong exponential dependence with temperature. This behavior of  $\rho_c$  can be described by an Arrhenius type equation, from which an activation energy of 0.35 eV for Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> and 0.26 eV for doped-Sb<sub>2</sub>Te is estimated. In the fully crystalline state  $\rho_c$  shows only a weak (linear) dependence with temperature (Fig. 4.8(b)).

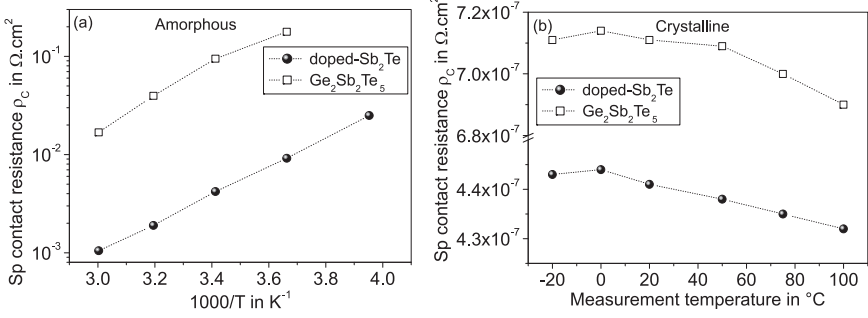


Figure 4.8: The temperature dependence of  $\rho_c$  values for TiW to doped-Sb<sub>2</sub>Te and Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> in the (a) amorphous and (b) crystalline states.

#### 4.1.5 Bias dependence of the contact resistance

The dependence of  $\rho_c$  on the sign and magnitude of the applied bias voltage is determined for TiW to doped-Sb<sub>2</sub>Te and TiW to Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> contacts with PCM in the amorphous and in the crystalline state. The contact resistance measurements were performed on CBKR structures with a PCM thickness of 20 nm and a contact area of  $1 \mu\text{m}^2$ . In this section from the derivative of the  $I$ - $V$  curve at the specified bias voltage,  $R_K$  is calculated and the value of  $\rho_c$  is extracted using eq. 2.10. The change in extracted  $\rho_c$  with positive and negative bias voltage across the contact in the amorphous and crystalline state of doped-Sb<sub>2</sub>Te and Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> is shown in Fig. 4.9 and Fig 4.10, respectively. The inset shows the corresponding current voltage ( $I$ - $V$ ) characteristics.

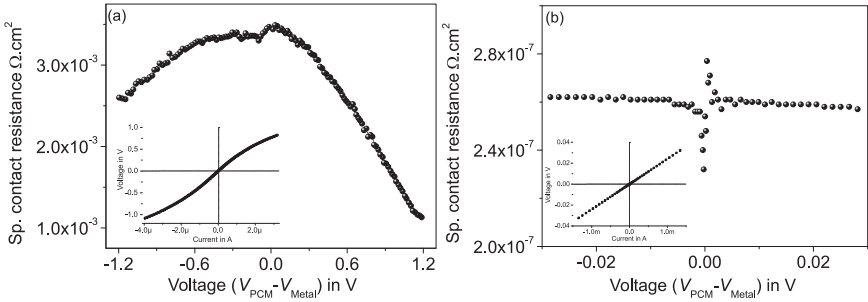


Figure 4.9: Change in  $\rho_c$  with applied bias voltage for TiW to doped-Sb<sub>2</sub>Te contacts; (a) amorphous state, (b) crystalline state. The inset represents the  $I$ - $V$  characteristics in the respective state of the PCM.

In the amorphous state non-linear  $I$ - $V$  characteristics is observed and the extracted  $\rho_c$  depends on the sign and magnitude of the applied bias. A positive measurement voltage ( $V_{\text{PCM}} - V_{\text{Metal}}$  positive) implies a higher potential on the

PCM side relative to the metal. Since PCM behaves like a  $p$ -type semiconductor material, with a positive potential the metal-PCM junction is forward biased. Hence with a larger positive bias the carriers can cross more easily from PCM to metal, resulting in a strong decrease in  $\rho_c$  values. With a negative potential at the contact, however the barrier for carriers moving from the metal to the PCM remains the same and a small change in  $\rho_c$  values are observed.

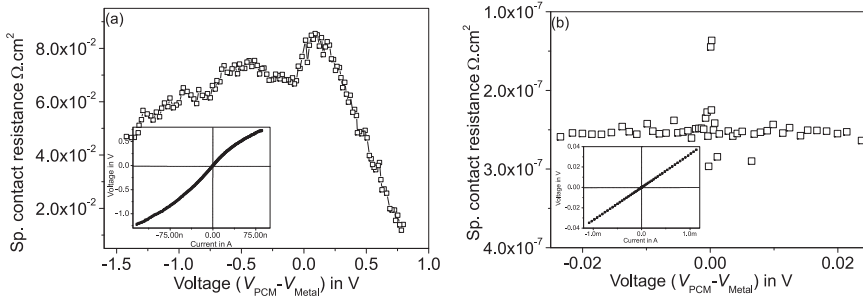


Figure 4.10: Change in  $\rho_c$  with applied bias voltage for TiW to  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  contacts; (a) amorphous state, (b) crystalline state. The inset represents the  $I$ - $V$  characteristics in the respective state of the PCM.

In summary, the results show a stronger dependence of  $\rho_c$  with positive bias compared to negative bias. This bias dependence of  $\rho_c$  is larger for  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ . For the crystalline state of the PCM, a linear  $I$ - $V$  is observed and  $R_K$  and  $\rho_c$  remain unchanged with the applied voltage bias.

### 4.1.6 Contact resistance with bias and temperature

The differences in the charge transport at the interface between metal electrode and amorphous or crystalline state of the PCM is discussed in the following sections. In the amorphous state of the PCM,  $\rho_c$  extracted for different bias voltages follows an exponential dependence with temperature. From this, Arrhenius type activation energy  $E_A$  can be calculated. This calculated  $E_A$  for different positive and negative voltage across the contact is shown in Fig. 4.11. The calculated  $E_A$  decreases with increase in positive voltage at the contact, while it remains almost constant for negative voltages. PCM is a  $p$ -type defect semiconductor. A positive potential means the metal-PCM junction is forward biased. At a larger positive bias, the barrier for charge carriers moving from PCM to metal is lowered. At a negative potential at the contact, the barrier for charge carriers moving from the metal to the PCM remains unaffected by the applied voltage. The estimation of barrier height from  $I$ - $V$ - $T$  measurements is in Appendix. A5.

If a barrier is formed at the metal-PCM interface, the carrier concentration ( $N_C$ ) at which the conduction mechanism changes from thermionic emission to tunneling can be determined based on the characteristic energy  $E_{00}$ , expressed

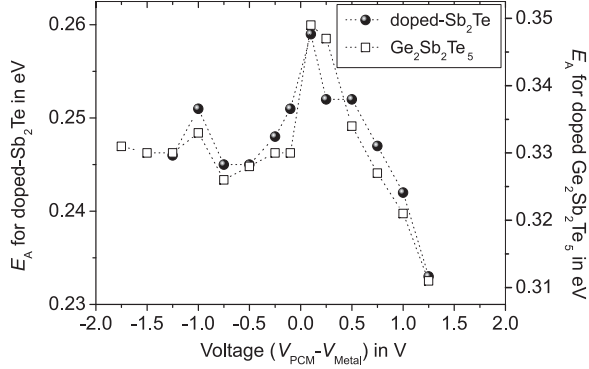


Figure 4.11: Calculated activation energy ( $E_A$ ) for positive and negative voltage bias across the contact with PCM in the amorphous state.

by eq. 2.4. The value of  $N_C$  and the mobility for both PCM's in the crystalline state is determined from Hall effect measurements (See Chapter 3.3). In the crystalline state of doped-Sb<sub>2</sub>Te, the measured carrier density is  $2 \times 10^{21} \text{ cm}^{-3}$  and the mobility is  $8 \text{ cm}^2/\text{V.s}$ . The calculated resistivity in the crystalline state is  $(36 - 45) \times 10^{-5} \Omega.\text{cm}$ , while in the amorphous state it is  $(15-21) \Omega.\text{cm}$ . That is a four orders of magnitude change in resistivity. The reported carrier mobility of PCM in the amorphous state is approximately  $0.1 \text{ cm}^2/\text{V.s}$  [77][8][78]. This means, as the PCM changes from crystalline to amorphous state, the resistivity increases by four orders in magnitude, while the mobility decreases by only two orders. Hence it is reasonable to assume that the carrier density also decreases by at-least two orders in magnitude. Using the reported dielectric constant ( $\epsilon_r$ ) for PCM of 17.7 in amorphous state and 38 in the crystalline state [79][80], the characteristic energy  $E_{00}$  can be calculated. This is given in Table 4.3 for doped-Sb<sub>2</sub>Te and Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub>. These calculations performed for the amorphous and crystalline state of PCM with tunneling electron mass  $m^*$  assumed equal to the electron mass  $m$  [81] and with  $m^*/m$  of 0.69 [82].

Table 4.3: Calculated  $E_{00}$  (eV) for metal to pcm contacts in the amorphous and crystalline states

Contact	Amorphous state		Crystalline state	
	$m^*/m=1$	$m^*/m=0.69$	$m^*/m=1$	$m^*/m=0.69$
Metal to doped-Sb <sub>2</sub> Te	0.02	0.024	0.134	0.162
Metal to Ge <sub>2</sub> Sb <sub>2</sub> Te <sub>5</sub>	0.008	0.01	0.05	0.063

For doped-Sb<sub>2</sub>Te in the amorphous state, the calculated value of  $E_{00}$  is in the range of  $k_bT$  (0.026 V at 300 K) suggests thermionic-field emission at the con-

tacts. For  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  an  $E_{00}$  value smaller than  $k_bT$  suggests thermionic emission as the major conduction mechanism at the contact. The bias and temperature dependence of  $\rho_c$  values measured for amorphous doped-Sb<sub>2</sub>Te show similarities with metal-semiconductors contacts for the case of thermionic-field emission: The  $\rho_c$  values are not symmetrical with the bias voltage and the resistance peak is not occurring at zero bias [83]. *The metal to amorphous PCM contacts show identical behavior to a metal to semiconductor contact with thermionic/thermionic-field emission as the main charge transport mechanism.*

In the crystalline state of the PCM, the calculated  $E_{00}$  values are larger than  $kT$ , indicating tunneling as the major conduction mechanism at the contact. In addition the extracted  $\rho_c$  values exhibit a weak dependence with the temperature and with the voltage bias. Given a similar carrier concentration of crystalline PCM, in the case of a metal to semiconductor contact shows ohmic behavior with a linear  $I-V$ . This is the condition where the tunneling process dominates [31]. It should be noted that the extracted  $\rho_c$  value is at least two orders of magnitude higher than common metal to metal contacts [63]. *The metal to crystalline PCM contacts show identical behavior as metal to doped semiconductor contacts with tunneling as the main charge transport mechanism.*

For regular semiconductors, the metal-semiconductor interfacial barrier height can be determined from the saturation current from current-voltage ( $I-V$ ) measurements, activation energy ( $I-V-T$ ) measurements, capacitance-voltage ( $C-V$ ) measurements or from photo current measurements. For metal to PCM contacts an exponential  $I-V$  characteristic is not obtained at a small region around zero. Hence saturation current cannot be determined accurately from these measurements (See Fig. 4.6). Measurements on capacitance structures show large leakage currents resulting in inaccurate measurements. Even though inaccurate, barrier height estimation from activation energy measurements (Richardson's plot) has been performed (see appendix A5). The extracted activation energy is slightly lower than the activation energy calculated from  $\rho_c$  shown in Fig. 4.11. As the calculated activation energy does not scale with the applied forward bias voltage determination of barrier height from these measurements is not valid.

## 4.2 Contact resistance with different metal electrodes

In the previous section TiW electrode to PCM contact resistance is systematically determined and expressed in terms of  $\rho_c$ . In this section the mechanism of interfacial barrier formation and the charge transport mechanism at the electrode to doped-Sb<sub>2</sub>Te interface are discussed. This is based on  $\rho_c$  measurements on Kelvin resistor structures (Fig. 2.2) realized with (CMOS compatible) electrodes of different work function. To fabricate these Kelvin resistor structures, first a 100 nm electrode layer is deposited by sputtering on an oxidized silicon wafer which is subsequently patterned to form the bottom electrode layer at the contact. A



500 nm PECVD  $\text{SiO}_2$  layer is then deposited and the wafer surface is planarized by Chemical Mechanical Polishing (CMP) down to the electrodes. Wafers were prepared with W, TiW, Ta, TaN and TiN electrodes. Process remnants and the native oxide layer on the electrode surface is removed by insitu sputter etching in argon plasma, and a 50 nm doped- $\text{Sb}_2\text{Te}$  is then deposited by sputtering, resulting in amorphous layers. This PCM layer is patterned with a maximum thermal budget of 90 °C to form the metal to amorphous PCM contact. The PCM in these structures were capped with a 25 nm evaporated  $\text{SiO}_2$  layer to protect against oxidation and evaporation during subsequent anneals.

Contact resistance measurements were performed on Kelvin resistor structures fabricated with these W, TiW, Ta, TaN and TiN electrodes. From these measurements on structures with different contact area,  $A$  the  $\rho_c$  is extracted using eq. 2.9. Measurements were performed on different dies annealed at different temperatures in the range 90 °C to 250 °C in an  $\text{N}_2$  atmosphere for 5 minutes. The PCM in the as-fabricated structures is in the amorphous state and will remain amorphous when annealed at temperatures less than 150 °C. The  $\rho_c$  of metal to amorphous doped- $\text{Sb}_2\text{Te}$  is extracted from the contact resistance measurements on these dies. Annealing at different temperatures in the range 175 °C to 250 °C transforms the PCM into the crystalline state. The  $\rho_c$  of metal to crystalline doped- $\text{Sb}_2\text{Te}$  is extracted from the contact resistance measurements on these annealed dies. The average extracted  $\rho_c$  from these measurements in the amorphous (a) and crystalline (b) state of doped- $\text{Sb}_2\text{Te}$  is shown in Fig. 4.12.

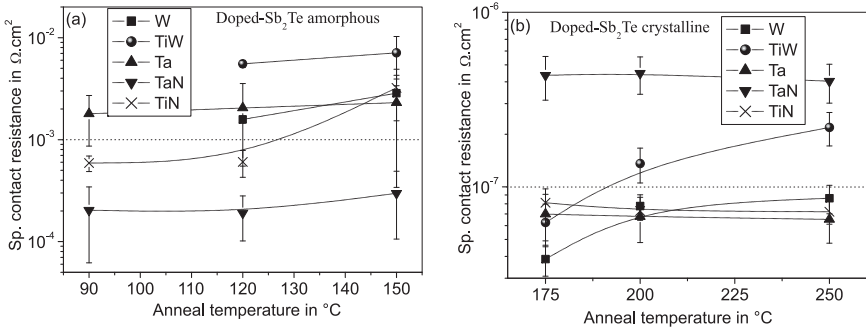


Figure 4.12: Change in extracted  $\rho_c$  as a function of annealing temperature in the amorphous (a) and in the crystalline (b) state of doped- $\text{Sb}_2\text{Te}$ .

The extracted  $\rho_c$  for metal to PCM depends on the state of the PCM and the metal electrode. The extracted  $\rho_c$  in the amorphous state is higher than in the crystalline state for all the metal electrodes. In the amorphous state of the doped- $\text{Sb}_2\text{Te}$ , metal nitrides electrodes (TaN and TiN) have a lower  $\rho_c$  as compared to metal electrodes (Ta, TiW and W). The lowest  $\rho_c$  ( $\approx 2 \times 10^{-4} \Omega \cdot \text{cm}^2$ ) is extracted for TaN and the highest  $\rho_c$  ( $\approx 5 \times 10^{-3} \Omega \cdot \text{cm}^2$ ) for TiW. The extracted  $\rho_c$  for all electrodes remain more or less constant when annealed up to 150 °C. The slight

increase when annealed at 150 °C could be due to the partial crystallization of PCM (explained in Ch. 6.2). In the crystalline state, the extracted  $\rho_c$  for both metal and metal nitrides is in the same range. The highest  $\rho_c$  is measured for TaN. For TiW and W, the extracted  $\rho_c$  with PCM in the crystalline state increases slightly with the annealing temperature. The change in extracted  $\rho_c$  with measurement temperature in the range of -40 °C to 40 °C for different electrode materials is shown in Fig. 4.13. These measurements are for doped-Sb<sub>2</sub>Te in the amorphous state (after 120 °C anneal) and in the crystalline state (after 200 °C anneal). In the amorphous state an exponential dependence is observed for  $\rho_c$  with temperature for all the electrodes, which is the energy required by the charge carriers to cross the interfacial potential barrier. The activation energy calculated for a TaN is 0.35 eV and for W is 0.254 eV. In the crystalline state  $\rho_c$  is almost independent of the temperature. From Fig. 4.12(a), a lower electrical

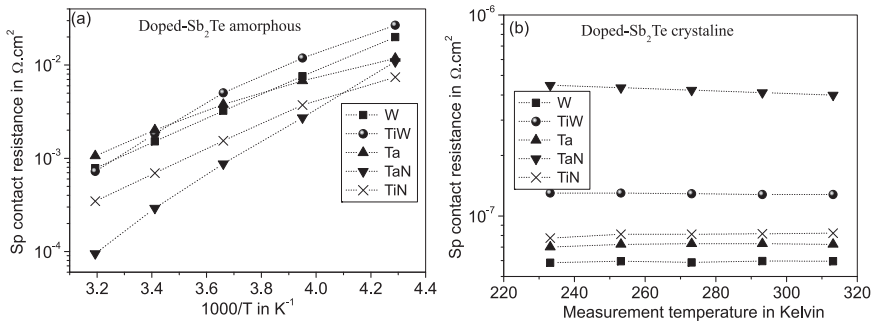


Figure 4.13: Change in extracted  $\rho_c$  with measurement temperature in the amorphous (a) and in the crystalline (b) state of doped-Sb<sub>2</sub>Te.

interfacial resistance is observed for metal-nitrides ( $\approx 10^{-4} \Omega \cdot \text{cm}^2$ ) as compared to the metal electrodes ( $\approx 10^{-3} \Omega \cdot \text{cm}^2$ ). In the case of pure metal electrodes, a chemical reaction is expected at the metal-PCM interface, which commonly results in a better defined and clean interface. On the other hand, in the case of metal nitrides, less chemical reaction is expected. The higher extracted  $\rho_c$  values for metal to amorphous doped-Sb<sub>2</sub>Te suggest that the electronic conduction is determined by the barrier formed and not by the material interaction at the interface.  $E_{00}$  calculations in Table 4.3 showed that charge transport through the metal to amorphous doped-Sb<sub>2</sub>Te interface is dominated by thermionic-field emission, which in-turn is dependent on the barrier height. A change in barrier height changes the contact resistance. In addition an exponential dependence of  $\rho_c$  is observed with temperature for all the electrodes. *This indicates that in the amorphous state the charge transport through the metal doped-Sb<sub>2</sub>Te interface is dominated by thermionic-field emission, which is dependent on the barrier height and temperature.*

In the crystalline state, the extracted  $\rho_c$  for both metal and metal nitrides is

in the same range ( $\rho_c \approx 10^{-7} \Omega.\text{cm}^2$ ). The highest  $\rho_c$  of  $\approx 5 \times 10^{-7} \Omega.\text{cm}^2$  is extracted for TaN electrode, while for W, Ta and TiN electrode extracted  $\rho_c$  is  $\approx 8 \times 10^{-8} \Omega.\text{cm}^2$ . In the case of TiW and W electrodes,  $\rho_c$  increases slightly when annealed at a high temperature. *In the crystalline state of doped-Sb<sub>2</sub>Te, the charge transport at the interface is dominated by tunneling and the extracted  $\rho_c$  is weakly dependent on the electrode metal (due to differences in barrier height)* [31]. In the crystalline state  $\rho_c$  is almost independent of the temperature which is also a characteristic of tunneling.

The electrode work function can be obtained from literature<sup>1</sup>. The resistivity of the electrodes can be calculated from associated Van der Pauw structures on the same wafer. The electrode work function and the resistivity values are shown in Table. 4.4.

Table 4.4: Measured resistivity and reported work function of the metals and metal nitrides

Electrode	Work Function in eV	Resistivity in $\mu\Omega.\text{cm}$
W	4.55	19.6±0.4
TiW	4.2	103.3±1
Ta	4.25	298.8±2.4
TaN	3.5	2327±27
TiN	3.7-4.1	218.1±2.4

The plot of extracted  $\rho_c$  with the work function of the metal electrode in the amorphous state (after 120 °C anneal) and in the crystalline state (after 200 °C anneal) of doped-Sb<sub>2</sub>Te is shown in Fig. 4.14.

With the PCM in the amorphous state, the extracted  $\rho_c$  increases with increase in electrode work function. PCM a defect material, behaves like a *p*-type semiconductor. For metal to *p*-type semiconductor contacts the interfacial barrier height decreases with increase in metal work function. A decrease in barrier height lowers the  $\rho_c$ . The opposite is true for an *n*-type semiconductor contact, where a lower work function metal decreases the barrier height and results in a lower  $\rho_c$ . As observed from Fig. 4.14(a), electrodes with a lower work function (metal nitrides) have a lower  $\rho_c$ . *Hence, metal to amorphous doped-Sb<sub>2</sub>Te contacts behave like a metal to n-type semiconductor contacts.* It is reported that the presence of donor states in the band gap alter the contact properties and show opposite

<sup>1</sup>The work function Ta is 4.25 eV, W is 4.55 eV [84] and for TiW is 4.2 eV [85][86]. The work function of sputter deposited metal nitrides TiN and TaN depends on nitrogen content, deposition conditions and also annealing condition after deposition. For these materials work function is obtained by comparing the reported resistivity with work-function. In the case of TiN with a  $\rho$  of 218  $\mu\Omega.\text{cm}$  the reported work function is between 3.7 eV to 4.1eV [87][88] [89]. For TaN without a high temperature anneal with a  $\rho$  of 2.3 m $\Omega.\text{cm}$  the work function is reported to be 3.5 eV [90].

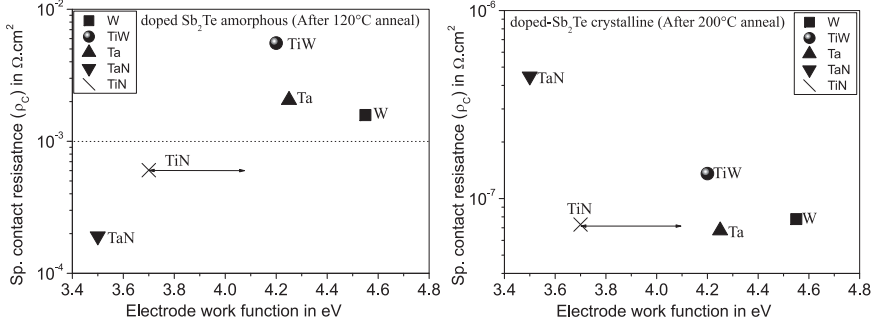


Figure 4.14: Change in  $\rho_c$  with metal work function for doped-Sb<sub>2</sub>Te in the amorphous and in the crystalline state. For TiN the arrow indicates the range of work function.

behavior. The presence of deep acceptor traps will increase the resistivity of the superficial layer and may even reverse the surface conductivity [91][92].

The  $E_{00}$  value calculated in the amorphous state of doped-Sb<sub>2</sub>Te suggests thermionic-field emission as the dominant charge transport mechanism across the interface. In this case, the  $\rho_c$  is described by eq. 2.8. Assuming the same pre-exponential factor for all the different electrodes, the difference in barrier height ( $\Delta\phi_b = \phi_{b1} - \phi_{b2}$ ) for two different electrodes can be calculated from the ratio of its  $\rho_c$  as:

$$\frac{\rho_{c1}}{\rho_{c2}} = \exp\left(\frac{q(\phi_{b1} - \phi_{b2})}{E_{00} \coth\left(\frac{E_{00}}{k_b T}\right)}\right) \quad (4.1)$$

The extracted  $\rho_c$  for the lowest available work function metal, TaN is  $1.9 \times 10^{-4} \Omega \cdot \text{cm}^2$  and for a highest work function metal, W is  $\rho_c$  of  $1.6 \times 10^{-3} \Omega \cdot \text{cm}^2$ . Using the thermionic-field emission model, the difference in barrier height calculated using eq. 4.3 for TaN and W is  $70.7 \text{ meV}^2$ . The actual value of Richardson's constant,  $A^*$  is not significant and it will be removed from the ratio. From Table. 4.4, the metal work function changes by approximately 1 eV. Based on the Schottky-Mott model in eq. 2.3, this change in metal work function should result in a change in the barrier height of the same order. *Apparently for metal to amorphous doped-Sb<sub>2</sub>Te interface, Schottky-Mott rule is not obeyed and the barrier height is not dependent on the metal work function. This could be due to the presence of interface defect states in amorphous doped-Sb<sub>2</sub>Te.*

In the crystalline state of the PCM, extracted  $\rho_c$  is almost independent of the metal work function as observed from Fig. 4.14(b). The largest  $\rho_c$  of  $4.5 \times 10^{-7} \Omega \cdot \text{cm}^2$  is extracted for TaN which has the lowest work function. *Metal to crystalline doped-Sb<sub>2</sub>Te contacts behaves like a metal to p-type semiconductor contact with the extracted  $\rho_c$  almost independent of the metal work function.*

<sup>2</sup> $\Delta\phi_b$  calculated using eq. 4.3 between TaN and TiW is 0.1 eV. Calculations with thermionic emission model also results in the same range of  $\Delta\phi_b$ .

## Donor/acceptor defects levels in amorphous doped-Sb<sub>2</sub>Te

For an ideal interface that is homogeneous, intimate, abrupt, and free from any structural or chemical defects, the barrier height is measured relative to the Fermi level given by eq. 2.3. Charge transfer takes place through the interface creating a contact potential (interface dipole), which is the difference between the two work functions. The total charge  $Q_M$  on the metal surface is compensated by an equal and opposite amount of charge  $Q_D$  on the PCM side of the interface. With the presence of defect states/interface states in the PCM, the total charge on the PCM side is the sum of the charges in the interface state and in the depletion region. The charge neutrality condition is  $Q_M + Q_D + Q_S = 0$ , where  $Q_S$  is the charge in the interface states.

Surface states created may be either interface defects [93] or Metal Induced Gap states (MIGS) [94]. The interface defects are created by either a vacant atomic site, disorder at the interface, dangling bonds, presence of impurities or foreign atoms, a thin oxide interfacial layer, or a chemical reaction or inter-diffusion at the interface. The metal-induced gap states (MIGS) model suggests that, for an intimate contact between metal and semiconductor, the metal wave functions are not abruptly terminated at the interface but extend far enough into the semiconductor to create states in its band gap. These states decay exponentially inside the semiconductor depending on the band gap.

In amorphous PCM, dangling bonds are considered to be point defects where the normal co-ordination is not satisfied. Depending on the atomic configuration of the dangling bond, a defect can have three charge states; neutral ( $D^0$ ) when occupied by one electron, negatively charged ( $D^-$ ) when occupied by two electrons and positively charged ( $D^+$ ) when unoccupied. A defect center can be donor like when negatively charged or acceptor like when positively charged [69][95][96]. The transfer of charge between two neutral defect is represented as  $2D^0 \rightleftharpoons D^+ + D^-$ . The energy difference between the left hand side and the right hand side is the correlation energy.

Amorphous chalcogenide is reported to have a negative correlation energy (negative  $U$  centers) [97][69][95]. This results in an equilibrium state which comprises of an equal density of  $D^+$  and  $D^-$  defects with no singly occupied states. Since the upper level is empty, and the lower level is filled,  $E_F$  must lie between the two energy levels [98]. The states below  $E_F$  are represented as donor like states ( $E_d$ ) and the states above  $E_F$  are represented as acceptor like states ( $E_a$ ). The resulting energy band diagram of amorphous PCM with valence band ( $E_V$ ) and conduction band ( $E_C$ ) separated by the band gap,  $E_g$  is shown in Fig. 4.15. The energy level at the interface at which the dominant character changes from donor like to acceptor like is represented as the level  $\phi_0$  [99]. This also represents the level  $E_{CNL}$ , below which the surface states should be filled for charge neutrality [94]. Energy considerations make it favorable for  $E_F$  to be located at  $E_{CNL}$ .

With the contact established, charge transfer takes place between the metal and the interface states within the band gap. Donor like states are neutral if

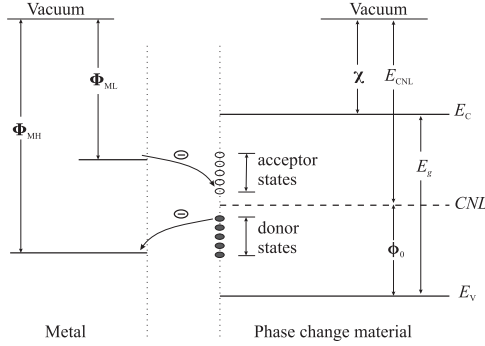


Figure 4.15: Energy band diagram of amorphous PCM showing the donor and acceptor defect states.

filled and are positively charged when ionized (unoccupied by electrons) while an acceptor states is neutral without an electron and negatively charged when ionized (occupied by an electron) [31][34]. When contacted with a high work function electrode material ( $\Phi_{MH}$ ), the neutral level  $E_{CNL}$  can be above  $E_F$ . Ionized empty donor states build up a large net positive interface charge as shown in Fig. 4.16 (a). Establishing a contact with a low work function electrode material ( $\Phi_{ML}$ ),  $E_{CNL}$  can be below  $E_F$ , excess electrons are transferred from the metal into the acceptor states in the PCM. Ionized occupied acceptor states lead to a net negative interface charge. The resulting energy band diagram is as shown in Fig. 4.16 (b).

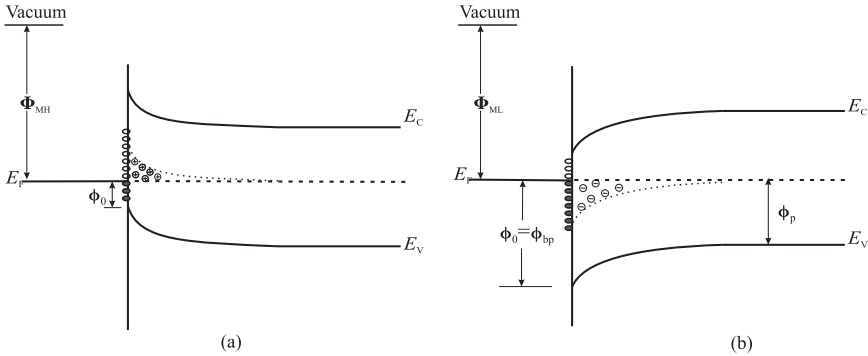


Figure 4.16: Band alignment between amorphous PCM with interface states and (a) high work function electrode ( $\Phi_{MH}$ ), (b) low work function electrode ( $\Phi_{ML}$ ).

In the case of PCM, charge carriers (holes) must be transported across the interface to establish conduction. A high work function electrode accumulates positive charge in the donor states at the interface. To maintain charge neutrality,

$Q_D$  will be greater than that without interface states. While a low work function electrode, accumulates negative charge at the interface and  $Q_D$  will be smaller than that without surface states. This results in the higher extracted  $\rho_c$  values for high work function metals compared to low work function metals. These localized donor and acceptor defect states situated in the band gap determines the electrical properties at the contact. The presence of interface states in the PCM creates a double layer, resulting from the surface charge in the interface states and in the space charge region. This double layer makes the barrier height independent of work function of the metal. This is called the Bardeen limit, where the barrier height is 'pinned' by the high density of interface states in the band gap. This results in the barrier height to be almost independent on the metal work function  $\Phi_M$  [99][94][100]. In this case,  $\Phi_M$  is replaced by effective work function ( $\Phi_{\text{eff}}$ ), which is the weighted average of the work function of the different interface states [101].

A strong Fermi level pinning is reported at the metal to PCM interface by x-ray photoelectron spectroscopy for different electrode materials [102][103][104][105].

In the case of Fermi-level pinning due to the presence of donor/accepter surface states which arise from unsatisfied dangling bonds or other defects on the semiconductor surface, de-pinning could be achieved by passivating those surface states [?]. This is not easily possible for phase change materials. MIGS created at the interface can be depinned by the introduction of a thin insulator layer at the interface [106][107][108]. Introduction of a thin oxide layer at the metal to PCM interface is reported to result in a lower contact resistance [18] and lower reset current in PCRAM cells [109]. Hence the creation of MIGS at the metal to PCM interface cannot be ruled out.

With the presence of interface states, the Schottky barrier height is represented as [110]:

$$q\phi_{bn} = S(\Phi_M - E_{\text{CNL}}) + (E_{\text{CNL}} - \chi) \quad (4.2)$$

$$q\phi_{bp} = S(E_{\text{CNL}} - \Phi_M) + (E_g + \chi - E_{\text{CNL}}) \quad (4.3)$$

where,  $S$  is the pinning factor which is experimentally obtained as [107]:

$$S = \frac{\partial\phi_b}{\partial\phi_M} \quad (4.4)$$

with  $S$  equals 1, describes the Schottky-Mott limit of no pinning with the barrier height described by the set of eq. 2.3, and with  $S$  as zero, describes the Bardeen limit of strong pinning due to the presence of large density of surface states. The barrier height is then represented as [111][94][26][110]:

$$q\phi_{bn} = E_g - \phi_0 = E_{\text{CNL}} - \chi \quad \& \quad q\phi_{bp} = \phi_0 = E_g + q\chi - E_{\text{CNL}} \quad (4.5)$$

By convention,  $\phi_0$  is measured from the valence band maximum and  $E_{\text{CNL}}$  measured from the vacuum level, but both of them effectively represent the same

energy level. In the amorphous state, Fermi level pinning is observed at the contacts due to the high density of donor/acceptor states in the PCM. This results in a weak barrier. Summarizing, based on the energy band diagram shown in Fig. 4.16(a) and (b), a high work function electrode results in larger  $\rho_c$  values and vice versa.

In annealed crystalline PCM, a neutral defect state (dangling bond) is energetically favorable [112][69]. Crystalline PCM is reported to have 20% of these vacant atomic sites exist in its lattice [113][96]. These structural vacancies in the material create acceptor like traps close to the valence band maximum, with the Fermi level close to this level [96]. Hall effect measurements on crystalline PCM, indicate p-type semiconductor properties. Due to the high density of these states, charge carriers tunnel through the interface resulting in an *ohmic* characteristic for crystalline PCM contacts.

### 4.3 Contact resistance of ultrathin PCM layers

In the case of a PCRAM line cell, writing current reduction is possible by controlling the PCM line resistance for maximum power transfer. This is possible by increasing the material resistivity by doping the chalcogenide layer, for instance with nitrogen [8] and also by controlling the geometry (thickness of the layer and width of the cell). The thickness of the chalcogenide layer can be controlled during the fabrication and is independent of the lithography limits. Reducing the film thickness leads to an increase of the cell resistance, decrease of the reset current and hence leads to a reduction in the current carrying capacity of the access transistor. Indeed, the thickness dependence of the switching properties of PCRAM cells shows that thinner layers have decreased power consumption [114]. In addition, crystallization temperature and crystallization rate [115][116] of the phase change materials have been studied with film thickness. Phase transformation from crystalline to amorphous and vice versa on the required timescales has been shown to be possible for chalcogenide layers as thin as 1.3-2 nm [8]. In this section, the effect of the layer thickness of the PCM (doped-Sb<sub>2</sub>Te) on the contact resistance is studied.

Contact resistance measurements were performed on Kelvin resistor structures fabricated with TiW electrode and with different thicknesses of the PCM layer. From these measurements,  $\rho_c$  is extracted using eq. 2.9. The extracted  $\rho_c$  with the contact area for various thicknesses of doped-Sb<sub>2</sub>Te in the amorphous and crystalline state is shown in Fig. 4.17. The extracted  $\rho_c$  is independent of the contact area for all thicknesses in the amorphous and crystalline states of the PCM. This indicates that in these structures the complete contact area is used for current transfer. In Fig. 4.17, the extracted  $\rho_c$  in the amorphous state for the thinnest layer is almost two orders in magnitude lower than for the thicker layer, whereas in the crystalline state there is hardly any influence of extracted  $\rho_c$  with the layer thickness. The dependence of the average  $\rho_c$  on the PCM thickness is



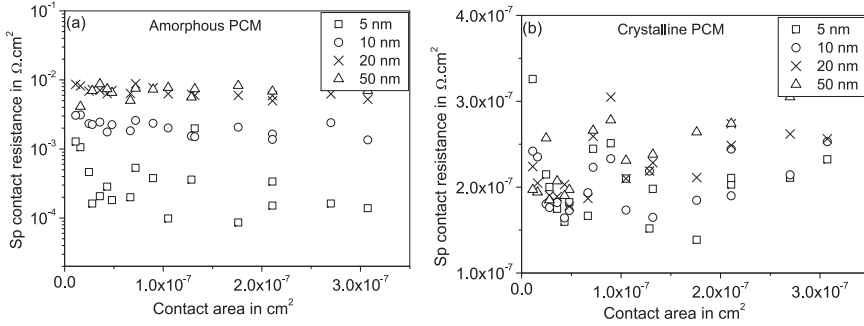


Figure 4.17: Extracted  $\rho_c$  with the contact area for different thickness of the doped-Sb<sub>2</sub>Te layer; (a) in amorphous state, (b) in the crystalline state.

shown in Fig. 4.18. In the amorphous state, the average  $\rho_c$  extracted for a 5 nm thick PCM layer is  $1.5 \times 10^{-4} \Omega \cdot \text{cm}^2$ , which increases to  $6 \times 10^{-3} \Omega \cdot \text{cm}^2$  for a thickness larger than 20 nm, while in the crystalline state, the extracted  $\rho_c$  is approximately  $2.5 \times 10^{-7} \Omega \cdot \text{cm}^2$  and independent of layer thickness. The change in extracted  $\rho_c$  with the measurement temperature in the range  $-40^\circ \text{C}$  to  $60^\circ \text{C}$  for different thickness of doped-Sb<sub>2</sub>Te in the amorphous state is shown in Fig. 4.18. An exponential dependence of  $\rho_c$  is observed with temperature for all the layers with almost the same slope.

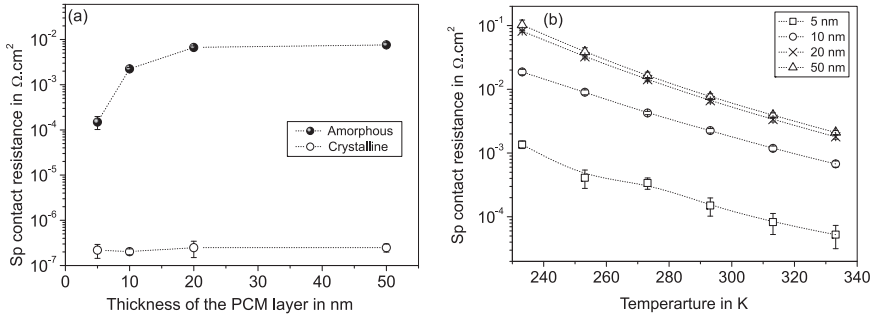


Figure 4.18: (a) Change in  $\rho_c$  with the thickness of doped-Sb<sub>2</sub>Te layer in the amorphous and crystalline states. (b) Change in  $\rho_c$  with the measurement temperature for different thickness of doped-Sb<sub>2</sub>Te in the amorphous state.

From accompanying Van der Pauw structures, the sheet resistance  $R_{\text{SH}}$  of the PCM layer is measured.  $R_{\text{SH}}$  is related to the resistivity  $\rho$  of the material by the eq. 2.28. The  $\rho$  calculated is  $15.09 \pm 0.2 \Omega \cdot \text{cm}$  for the amorphous state and  $364.4 \pm 9.5 \mu\Omega \cdot \text{cm}$  for the crystalline state. In our case,  $\rho$  is independent of thickness  $h$  in the range of 5-50 nm. The calculated transfer length using eq. 2.12 and  $R_{\text{SH}}$  from Van der Pauw measurements for the thinner amorphous PCM

layers indicate that the complete contact area is not used for the current transfer. However, the measurements in Fig. 4.17, shows that the contact is completely used for current transfer. This suggests that the PCM at the contact in these Kelvin structures is modified or has a different electrical properties compared to PCM in the Van der Pauw structures.

When PCM, a low mobility defect semiconductor, is brought into contact with a metal, charge transfer takes place through the interface to bring the Fermi levels into alignment. This results in an interface dipole which prevents further charge transfer and results in a modified region at the interface. This existence of a modified (depleted or accumulated) region in different chalcogenide materials at the interface with metals has already been postulated earlier [117][118][119].

Assuming a semiconductor model, the width of this modified region  $x_d$  is given by [120]:

$$x_d = \sqrt{\frac{2\phi_i\epsilon_s}{qN_C}} \quad (4.6)$$

where,  $\phi_i/q$  is the built in voltage at the space charge region (which is the work function difference between metal and PCM),  $\epsilon_s$  ( $= \epsilon_0\epsilon_r$ ;  $\epsilon_0 = 8.85 \times 10^{-14}$  F/cm) is the permittivity of the PCM and  $N_C$  is the charge carrier density.

In the crystalline state of the PCM, the reported dielectric constant ( $\epsilon_r$ ) is 38 [79] and our measurements show an  $N_C$  of  $2 \times 10^{21}$  cm<sup>-3</sup> and mobility of 8 cm<sup>2</sup>/V.s. Using this, the width of the space charge region is calculated to be 0.55 nm. The value of  $\phi_i$  for TiW to PCM interface is assumed to be 0.1 eV [117]. Given this carrier density and depletion width, the charge transport at a metal to semiconductor contact is dominated by tunneling and  $\rho_c$  remains independent of layer thickness. In the amorphous state, the carrier density changes (decreases) by at-least two orders in magnitude (See section 4.2). Given the reported dielectric constant ( $\epsilon_r$ ) of approximately 17.7 for the PCM in the amorphous state [80][79], the width of the modified region  $x_d$  is calculated to be 5.3 nm. This is in the same order as the lowest thickness of doped-Sb<sub>2</sub>Te studied in this work, from which a lower  $\rho_c$  is extracted in the amorphous state of the PCM.

The space charge region formed creates a barrier for charge transport at the contact. In the case of crystalline semiconductors, information about this barrier, surface states and screening length can be obtained from  $I$ - $V$  characteristics, frequency dependent capacitance-voltage measurements, or contact surface photo voltage measurements. In the case of metal to amorphous chalcogenide contacts, it is rather difficult to estimate the barrier height from any of these techniques [118]. When illuminated, additional charge carriers are generated in the modified region and in the rest of the layer. These photo-generated carriers in the modified region change the internal field in this region. At a metal PCM contact, this changes the contact resistance. Charge carriers generated outside this region follow the external field if applied. Hence the existence of a modified region at the interface can be investigated by electrical measurements on Kelvin structures with and without illumination.

It has been reported that in chalcogenides, radiation effects do not result in any permanent changes in the material structure. It only results in the generation of charge carriers [119]. As light propagates through the material the intensity decreases exponentially due to absorption [119]. This is characterized by the absorption coefficient,  $\alpha$ , the inverse of which is the average distance travelled by the photon before it gets absorbed.  $\alpha$  is obtained from the extinction coefficient,  $k$ . The  $k$  and  $\alpha$  values for doped-Sb<sub>2</sub>Te for a wavelength ( $\lambda$ ) range of 300 nm to 700 nm are shown in Table 4.5.

Table 4.5: Range of  $\alpha$  and  $k$  for white light

$\lambda(\text{nm})$	$k$	$\alpha(\text{cm}^{-1})$	$\alpha^{-1}(\text{nm})$
300	2.26	$9.5 \times 10^5$	10.6
400	2.89	$8.85 \times 10^5$	11.3
700	2.29	$4.11 \times 10^5$	24.3

To investigate the existence of a modified region at the TiW to doped-Sb<sub>2</sub>Te interface,  $I$ - $V$  measurements were performed on Kelvin structures with and without light exposure. Fig. 4 shows the result of these measurements performed on the Kelvin structures with 5 nm, 10 nm, 20 nm, and 50 nm thick doped-Sb<sub>2</sub>Te in the amorphous state. As shown in Fig. 4.19, the  $I$ - $V$  characteristics in these measurements changes from an asymmetric non-linear pattern to an almost linear pattern with increasing PCM thickness. In the case where measurements were performed in dark, the  $I$ - $V$  characteristics for Kelvin structures with a 5 nm doped-Sb<sub>2</sub>Te layer show significant asymmetry. In these structures, doped-Sb<sub>2</sub>Te is on top of the metal and is not capped with SiO<sub>2</sub>. When exposed to light, it will first enter the PCM. As shown in Table 4.5, the maximum characteristic length over which visible light is absorbed in amorphous doped-Sb<sub>2</sub>Te is 24 nm. The exponential decrease in intensity of the light with the distance generates only a small amount of photon at the maximum depth. The measured voltage,  $V$ , on the Kelvin structures is independent of current and it is the average potential drop across the contact. In the case of thinner layers, the PCM is modified down to the metal. In addition, if the light reaches the metal at the contact it will be reflected, creating additional absorption in the PCM. As observed from Fig. 4.19, for 5 nm layers the  $I$ - $V$  characteristics changes significantly with the application of light and the measured voltage at the contact decreases. However for the thicker layers, light modifies the PCM regions only far from the contact and hence, a small effect is observed in the contact potential. This indicates that modification of the PCM close to the interface influences the contact resistance confirming the existence of a region in the amorphous PCM close to the interface with different properties compared to the film. This explains the lower extracted  $\rho_c$  values for thinner layers. In the case of crystalline PCM layers linear  $I$ - $V$  characteristics are observed, insensitive to light.

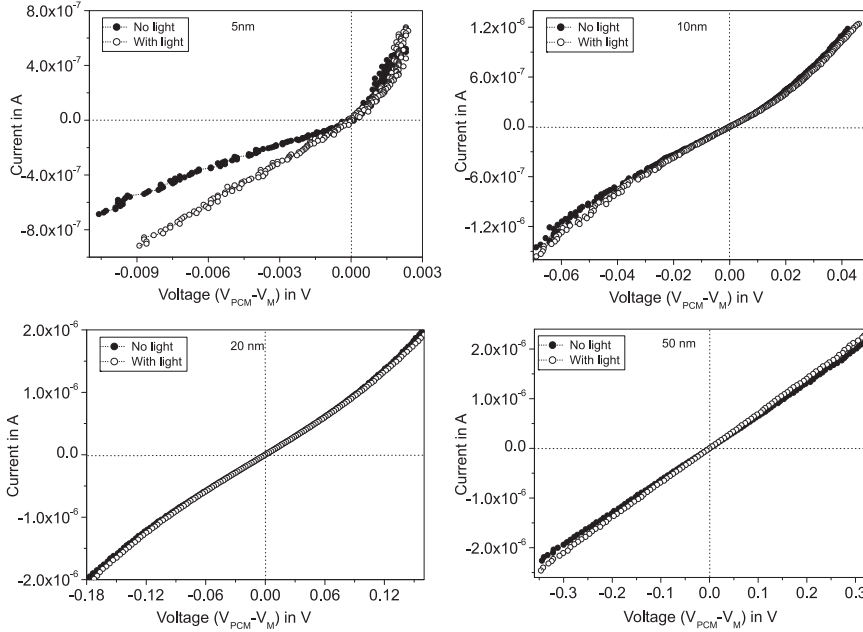


Figure 4.19: Change in current-voltage characteristics measured on Kelvin structures with and without illumination for 5 nm, 10 nm, 20 nm, and 50 nm doped-Sb<sub>2</sub>Te in the amorphous state.

## 4.4 Conclusions

In this chapter the electrode to PCM contacts are electrically characterized and modeled. The electrical resistance measurements performed on identical contacts from Kelvin resistor method (CBKR) structures and Transfer Length Method (circular-TLM) test structures resulted in similar  $\rho_c$  values for amorphous and crystalline PCM. Contacts to growth dominated doped-Sb<sub>2</sub>Te and nucleation dominated Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> were studied. In combination with measurements for different CMOS compatible electrodes (W, TiW, Ta, TaN and TiN) the charge transport at the electrode to doped-Sb<sub>2</sub>Te interface is modeled.

The extracted  $\rho_c$  for TiW to amorphous doped-Sb<sub>2</sub>Te is approximately  $10^{-3} \Omega \cdot \text{cm}^2$  and for TiW to amorphous Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> is approximately  $10^{-2} \Omega \cdot \text{cm}^2$ . The extracted  $\rho_c$  for metal nitride electrodes to doped-Sb<sub>2</sub>Te ( $\rho_c \approx 10^{-4} \Omega \cdot \text{cm}^2$ ) is lower than for the corresponding metal electrodes ( $\rho_c \approx 10^{-3} \Omega \cdot \text{cm}^2$ ). In the crystalline state of the PCM, a  $\rho_c$  value of approximately  $2 \times 10^{-7} \Omega \cdot \text{cm}^2$  is extracted for TiW electrode to doped-Sb<sub>2</sub>Te and Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub>. They do not show any dependence with the work function of different electrode, and the values are in the same range ( $\rho_c \approx 10^{-7} \Omega \cdot \text{cm}^2$ ). When measured with different thickness of the amorphous doped-Sb<sub>2</sub>Te layer, the average extracted  $\rho_c$  increases from

$1.5 \times 10^{-4} \Omega.\text{cm}^2$  for a 5 nm thick PCM layer to  $6 \times 10^{-3} \Omega.\text{cm}^2$  for a thickness larger than 20 nm. In the crystalline state the extracted  $\rho_c$  remains constant, which is approximately  $2.5 \times 10^{-7} \Omega.\text{cm}^2$ .

In the amorphous state,  $\rho_c$  values show a strong exponential dependence with measurement temperature. In addition a stronger dependence of  $\rho_c$  values with positive bias is observed as compared to negative bias. These measurements and the calculated  $E_{00}$  values based on the material parameters derived from the previous chapter, it is concluded that the charge transport at the metal to amorphous doped-Sb<sub>2</sub>Te interface is dominated by thermionic-field emission. The interface barrier formation at a metal to amorphous doped-Sb<sub>2</sub>Te interface is modeled with the presence of donor like and acceptor like defect states created in the PCM. Measurements performed on Kelvin structures with ultra-thin doped-Sb<sub>2</sub>Te layers indicated the existence of a modified region in the PCM at the interface, which is attributed to the dependence of  $\rho_c$  on the layer thickness. In the crystalline state, the extracted  $\rho_c$  is almost independent on the measurement temperature as well as on polarity of applied bias voltage. The measurements presented in this chapter and the calculated  $E_{00}$  values, indicate that tunneling is the main charge transport mechanism at a metal to crystalline PCM interface. The electrical properties of the metal to PCM contacts in both states show close similarities with the metal to semiconductor contacts.



## High frequency contact resistance measurements

During operation, the current enters and exits through the contacts to the functional layers in a device. Depending on the nature and operation of the device, current may flow continuously (DC) or for short intervals (HF) through the contacts. Hence, during operation, the potential at the contacts may remain static or is dynamic with time. For complete understanding of the contact, the  $\rho_c$  values at its operating frequency range is essential.

In this chapter, the (Scott and linear) TLM structure is modified and a novel data extraction procedure is presented, that is suitable for contact resistance measurements at high frequencies. From the measurements on these structures the  $\rho_c$  values are extracted with signal frequencies up to 4 GHz. This chapter starts by explaining the relevance of high frequency contact resistance measurements for PCRAM cells. In the subsequent section, the design requirements and fabrication steps for test structures are presented. Use of different interface treatments during fabrication resulted in TiW to crystalline doped-Sb<sub>2</sub>Te contacts with different  $\rho_c$  values. In the following sections, the contact resistance measurements with frequency from modified Scott TLM and linear TLM structures are presented. The frequency dependence of the contacts is electrically modeled with a resistance-capacitance network. Scott TLM structures have contacts with varying contact area while linear TLM structures have a fixed contact area, which is visible in the extracted interface capacitance values.

## 5.1 Relevance of high frequency contact resistance measurements

PCRAM cells often consist of a thin-film of chalcogenide alloy or PCM layer integrated into the metallization level of the integrated circuit [7]. The principle of operation of these cells is based on the switching of this PCM layer between the amorphous (reset state) and the crystalline (set state) phase. Typically set, reset or read operation of the cell are achieved using different electrical pulses of nano-second duration [7][121]. Phase change memory cells have been demonstrated for very fast material switching times down to 1 ns for both set and reset operation [122]. A PCRAM cell with 2 ns read-time is reported to allow up to 200 MHz data throughput [121]. Furthermore, research is progressing to improve the electrical switching speed of PCM, which has been demonstrated to switch with pico-second laser pulses [123]. With these improved switching speeds, a PCRAM cell can operate at even higher data throughput rates.

Electrical current flows through the memory cell only when it is accessed for either set, reset or read operation. Hence, during operation of the device, the electric potential at the contacts follows this fast changing signal. Metal to PCM contact resistance measurements and  $\rho_c$  values reported in Chapter 4 are obtained from static DC current and voltage signals. For complete understanding of the performance of a PCRAM cell, the contacts of which follows a fast changing (dynamic) signal, the properties of the contacts at its operating frequency range is crucial. In this chapter, Scott TLM structures and the linear TLM structure are modified and a novel data extraction procedure is presented, which is suitable for interface characterization at High Frequencies (HF). Two port S-parameter measurements were performed on these structures, from which metal to PCM contact impedance and  $\rho_c$  is extracted as a function of frequency (up to 4 GHz). These extracted contact parameters are validated with the values measured at DC using identical four point test structures. The frequency dependence of the contact interface is electrically modeled with an interface resistance and capacitance network. Finally, based on the measurements the model parameters are extracted for different  $\rho_c$  values.

With the presence of parasitic capacitances at the contact, the application of a step-function bias results in a transient current response [124]. The presence of parasitic capacitance is shown to influence the transistor circuit performance [125]. It was also shown that the presence of the electrode to substrate parasitic capacitance can influence the programming performance of PCRAM cells at high frequencies [126]. The measurements presented in this chapter deal with the characterization of the electrode to PCM interfacial capacitance. The uniqueness of contact resistance measurement with frequency is that, these measurements can identify and separate this interfacial capacitance from the interfacial resistance. Attempts to extract the interfacial capacitance with voltage at a Schottky contact have also been reported [127][128].



## 5.2 Test structure and measurements

Scott TLM structures (in Fig. 2.9) and linear TLM (in Fig. 2.6) structures were fabricated in the Ground-Signal-Ground (GSG) configuration to facilitate HF measurements. To validate these measurements, identical TLM structures should be available both in GSG configuration (HF measurements) and four bond-pad configurations (DC measurements). A SEM image of a Scott TLM structure in both the configurations is shown in Fig. 2.11. In order to increase the measurement accuracy it is important to match the characteristic impedance of the test structure with the measurement equipment source/load impedance, which is typically  $50 \Omega$ . This is adjusted by the number of squares (unit area) of the PCM layer in the measurement structure. In addition, for each TLM structure an open circuit and short circuit de-embedding structure is required. These de-embedding structures are essentially the same GSG TLM structure, however for the open calibration structure the PCM layer is not present and for the short calibration structure the PCM layer is replaced by a very low resistive aluminium line.

Two port S-parameter measurements were performed in the frequency range from 1 MHz to 4 GHz on GSG TLM test structures using an Agilent E5071C network analyzer. The analyzer is first calibrated up to the probe-tips using a Short-Open-Load-Thru (SOLT) calibration. To remove the influence of the bond pads and interconnects in the test structure, the dedicated open and short de-embedding structures are measured [129][130]. Then from the measured S-parameters after calibration and de-embedding, the real and the imaginary part of the differential impedance ( $Z$ ) offered by each structure is calculated using eq. 2.26. The contact impedance ( $Z_C$ ) is calculated from  $Z$ . The DC electrical resistance of the structure is obtained from the current voltage measurements performed using an HP 4155C semiconductor parameter analyzer.

### Test structure fabrication

HF test structures, calibration structures and DC measurement structures were processed on the same oxidised silicon wafer. To fabricate these test structures, first, a 100 nm TiW layer is sputter deposited and patterned to form the bottom electrode layer in the TLM structures. For Scott structures it is required to have metal segments of equal length distributed at constant pitch. To pattern these metal segments first a resist mask is created on the metal by photo lithography. Then this resist mask pattern is transferred to the metal by reactive ion etching. Changing the exposure energy during lithography changes the dimensions of the resist mask pattern and hence the dimensions of the metal segments. To meet the design requirement of the Scott structures, the exposure energy is optimised by creating a "focus exposure matrix" wafer. Different dies in this wafer are exposed with increasing energies of a fixed step size. After exposure the photo resist is developed and the metal is etched. The dimensions of the metal segments after etching was measured using a SEM. Fig. 5.1 shows the change in length of

the metal segments,  $L_i$  and spacing with exposed energy in the range from  $190 \mu\text{J}/\text{cm}^2$  to  $240 \mu\text{J}/\text{cm}^2$ .

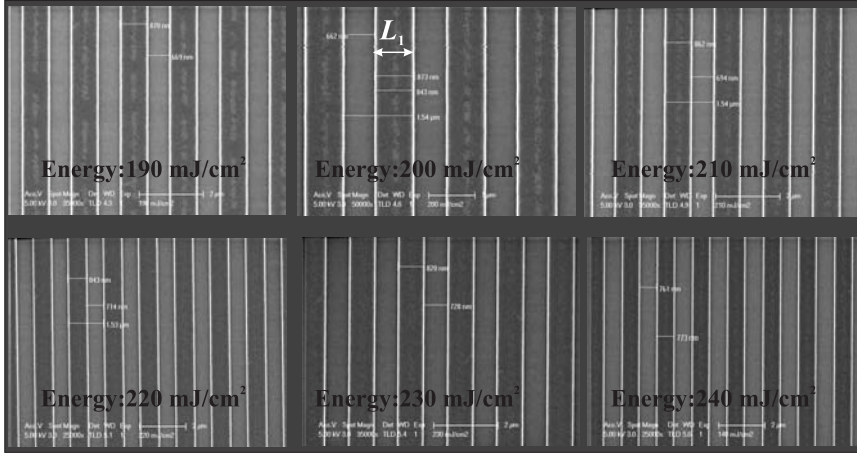


Figure 5.1: Change in  $L_i$  pitch of the metal segments with exposure energy for Scott TLM structure S6.

The change in  $L_i$  and spacing between metal segments with exposure energy for three Scott TLM structures S5, S6 and S7 is shown in Fig. 5.2. With constant

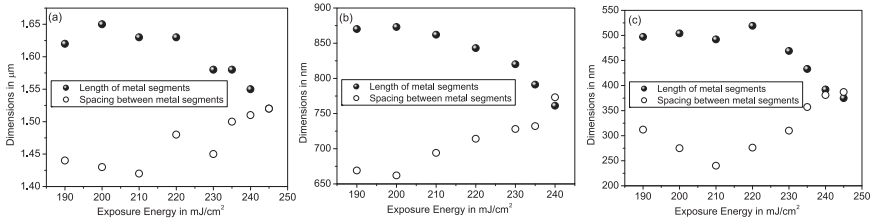


Figure 5.2: Change in  $L_i$  and the spacing between metal segments with exposure energies used for Scott structure S5, S6 and S7.

pitch for the metal segments,  $L_i$  decreases when exposed at higher energies used. Considering the limiting condition for the Scott structures, to have equal  $L_i$  and the spacing between the metal segments, an exposure energy of  $240 \mu\text{J}/\text{cm}^2$  is used in the fabrication of the test structures.

Once the metal segments are formed, the wafer surface needs to be planarized to obtain a uniform PCM line. For this, a 500 nm PECVD  $\text{SiO}_2$  layer, (greater than three times the step height), is deposited at  $400^\circ\text{C}$  and then the wafer surface is planarized by Chemical Mechanical Polishing (CMP) to remove the  $\text{SiO}_2$  from the TiW surface [131]. Metal dishing or oxide erosion effects [132] of the type shown Fig. 5.3 may occur during the CMP. To limit these effects, a dense

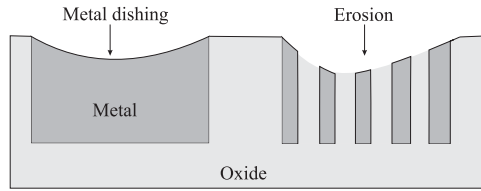


Figure 5.3: Dishing and erosion effects during CMP

metal pattern is required and hence, metal tiles have been designed and included in the open spaces around the structures [133]. These metal tiles included around the Scott structure are shown in Fig. 2.11. Cross sectional SEM images of realized buried metal segments of three different lengths are shown in Fig. 5.4.

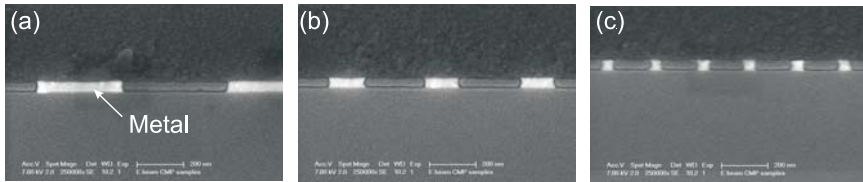


Figure 5.4: Cross-section SEM images of the metal segments after CMP

A 500 nm aluminium layer is then sputter deposited and patterned to form the ground lines to reduce the ground impedance between the ports, and the bond pad regions to facilitate probing. Finally, a 50 nm PCM layer is deposited by sputtering and patterned to form the metal to PCM contacts in these structures. Three different wafers were fabricated with these test structures having different surface treatments before PCM deposition and patterning. The first wafer (wafer-1) is fabricated with Ar pre-clean (sputter-clean) before PCM deposition. This Ar pre-clean step removes all the process remnants and native oxide from the metal surface resulting in a good metal to PCM interface [134]. For the second (wafer-2) and third wafer (wafer-3) the Ar pre-clean step is omitted, and for wafer-3, an additional treatment was done in oxygen plasma at 110 °C for 5 min (descum). Here an interfacial layer is introduced intentionally between metal and PCM. In the case of wafer-3 an even thicker oxidised interfacial layer is expected. The fabrication differences of the three wafers are summarised in Table 5.1. Prior to measurements, these structures were annealed at 200 °C for 5 min in a N<sub>2</sub> atmosphere. This transforms the PCM in these wafers to the crystalline state.

Table 5.1: Fabrication details of the three wafers

Fabrication Step	Wafer-1	Wafer-2	350 Wafer-3
O <sub>2</sub> descum	No	No	Yes
Ar pre-clean	Yes	No	No

### 5.3 Scott-TLM measurements

In this section, the DC measurements and HF measurements performed on Scott TLM structures are presented. These measurements were performed on structures fabricated on all three wafers with different interface treatments. Scott TLM structures were available with a PCM line width of 50  $\mu\text{m}$ , 20  $\mu\text{m}$ , 10  $\mu\text{m}$ , 5  $\mu\text{m}$ , 2  $\mu\text{m}$ , and 1  $\mu\text{m}$ . Test structures were available with  $L_i$  varying from 25  $\mu\text{m}$  to 390 nm as given in Table 2.1.

#### 5.3.1 DC measurements

From the measured resistance of each structure, the total contact resistance,  $R_{CT}$  and the resistance per contact,  $R_C$  is calculated using eq. 2.20 and 2.21 respectively. Fig. 5.5(a) shows the dependence of normalised resistance ( $R_C W$ ) per contact with  $L_i$  for three different width,  $W$  of the PCM layer. These measurements are for wafer-3 (with descum and no Ar pre-clean). Based on these measurements the plot of eq. 2.24 with  $L_i$  is derived as shown in Fig. 5.5(b). From the slope of this curve, a transfer length ( $l$ ) of 6.2  $\mu\text{m}$  and using eq. 2.12, a  $\rho_c$  value of  $3.2 \times 10^{-5} \Omega \cdot \text{cm}^2$  are calculated.

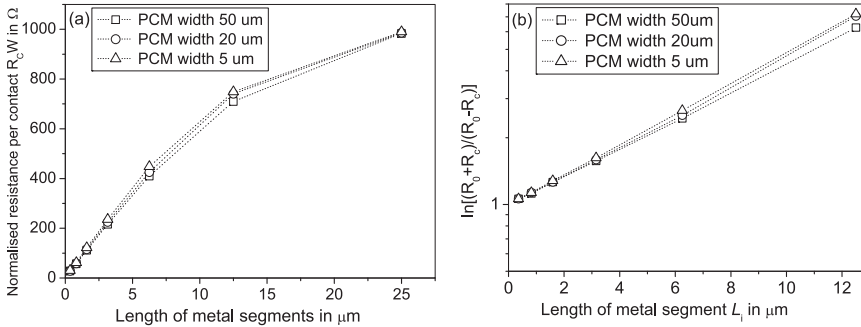


Figure 5.5: Plot of (a)  $R_C W$  with  $L_i$  (b) limiting condition of the contact resistance (eq. 2.24) with  $L_i$  for wafer-3

Similar measurements performed for wafer-2 result in an  $l$  of 3.2  $\mu\text{m}$  and  $\rho_c$  of  $8.8 \times 10^{-6} \Omega \cdot \text{cm}^2$ , and for wafer-1 results in an  $l$  of 250 nm and  $\rho_c$  of approximately  $8 \times 10^{-8} \Omega \cdot \text{cm}^2$ . The fit derived for  $R_C$  based on this extracted  $\rho_c$  and  $R_{SH}$  values

and using eq. 2.22 is shown in Fig. 5.6. These measurements are for the Scott structures with PCM width of  $20 \mu\text{m}$ . The  $R_{\text{SH}}$  of the PCM layer is measured using Van der Pauw structures, which is approximately  $70 \Omega/\square$  for all three wafers. The measured  $R_C$  and calculated fit shows good agreement for all the three wafers.

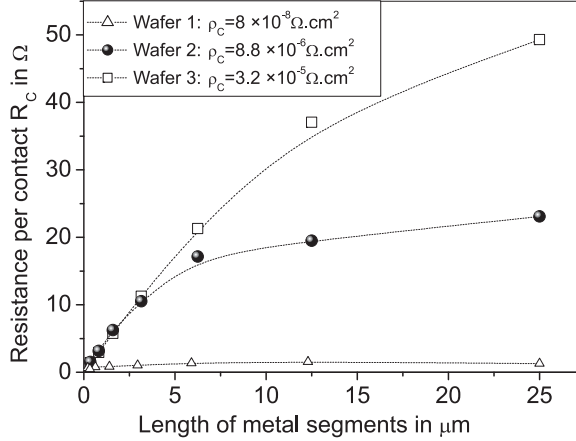


Figure 5.6: Plot of  $R_C$  with  $L_i$  for all three different wafers. The extracted  $\rho_c$  from these measurements is also indicated. The symbols  $\bullet$ ,  $\square$ , and  $\triangle$  represent the measured points and the line represents the derived fit.  $W$  is  $20 \mu\text{m}$ .

Wafer-1 has a clean metal to PCM interface. This resulted in the lowest extracted  $\rho_c$ , while wafer-3 which has an oxidised interface, resulted in the highest  $\rho_c$ . In this case, the presence of an interfacial layer creates an additional barrier at the interface.

### 5.3.2 High frequency measurements

The real and the imaginary parts of the differential impedance  $Z$ , offered by each Scott TLM structure is calculated using eq. 2.26 from its measured S-parameters. Then, by deducting the impedance of the reference structure from the measured impedance  $Z$  using eq. 2.20, the real and the imaginary part of the total contact impedance  $Z_{\text{CT}}$  offered by each Scott structure is calculated. The calculated real part of  $Z_{\text{CT}}$  ( $\text{Re}\{Z_{\text{CT}}\}$ ) and the imaginary part of  $Z_{\text{CT}}$  ( $\text{Im}\{Z_{\text{CT}}\}$ ) for Scott structure S1 with only one metal segment are shown in Fig. 5.7 for all three wafers. Hardly any frequency dependence is observed for the real and the imaginary part of  $Z_{\text{CT}}$  for wafer-1. In the case of wafer-2 and wafer-3, both real and imaginary part of  $Z_{\text{CT}}$  do show a frequency dependence. The resistance measured at DC;  $1.9 \Omega$  for wafer-1,  $23.1 \Omega$  for wafer-2 and  $51 \Omega$  for wafer-3. This is consistent with the measurements at 1 MHz shown in Fig. 5.7. In Scott

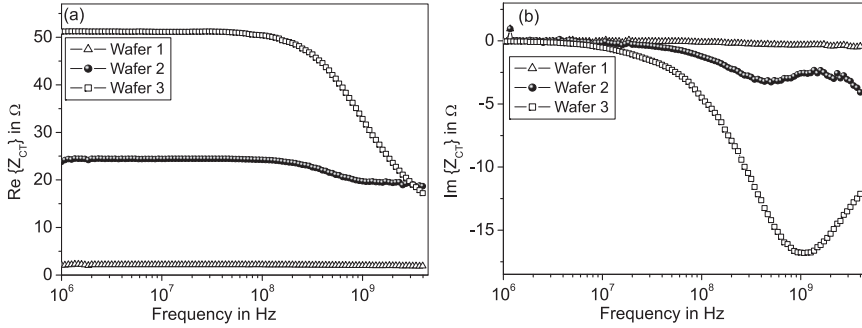


Figure 5.7: (a) Comparison of frequency dependence of  $Z_{CT}$  of Scott structure S1 for all three wafers. (a) Real part of  $Z_{CT}$ , (b) imaginary part of  $Z_{CT}$ .

structure S1 (one metal segment) the total contact impedance  $Z_{CT}$  is the same as the contact impedance per metal segment  $Z_C$ . From the measured impedance of Scott structures (S2-S7), the value of  $Z_C$  can be calculated assuming eq. 2.21. The change in calculated  $\text{Re}\{Z_C\}$  with the length of the metal segments at different frequencies for wafer-3 is shown in Fig. 5.8(a). The measured value at DC is also shown. From these measurements,  $\rho_c$  is extracted using eq. 2.25. In Fig. 5.8(b), the extracted  $\rho_c$  with frequency is shown for wafer-2 and wafer-3.

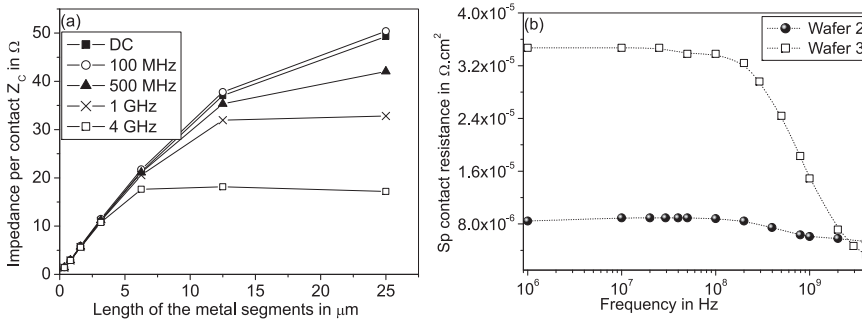


Figure 5.8: (a) Change in  $\text{Re}\{Z_C\}$  with the length of the metal segments for wafer-3 measured at different frequencies, (b) extracted  $\rho_c$  for wafer-2 and wafer-3 with frequency.

In the case of wafer-1, the extracted  $\rho_c$  of  $8 \times 10^{-8} \Omega.\text{cm}^2$  is independent of the frequency. Wafer-2 and wafer-3 had an intentionally formed interfacial layer between the metal and the PCM. This interfacial layer acts like a capacitor at the contact resulting in a frequency dependent behaviour. In the case of wafer-3 the thicker interfacial layer results in the relatively prominent frequency dependence. A capacitive interface when measured with frequency, shows a visible change in the measured impedance when the real part of the contact impedance equals the

imaginary part of contact impedance.

### 5.3.3 Contact model

The frequency dependence of the metal to PCM interface can be electrically modelled as a resistance  $R_{CS}$  in series with a parallel combination of a capacitor  $C_{CP}$  and a resistor  $R_{CP}$ . The contact interface is modelled as shown in Fig. 5.9:

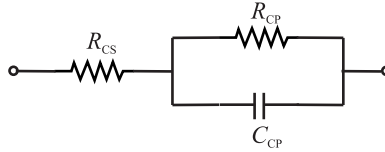


Figure 5.9: Electrical model of metal to PCM interface.

The series resistance  $R_{CS}$  is the interfacial contact resistance formed due to the difference in work function of the two materials at the contact. The interface capacitor  $C_{CP}$  is formed due to the presence of the interfacial layer at the contact (only for wafer-2 and wafer-3). The resistor  $R_{CP}$  accounts for the leakage through  $C_{CP}$ . The same model has been proposed for metal-semiconductor contacts [135][136].

The electrical contact model for an individual metal segment with  $L_i$  much greater than  $l$  is shown in Fig. 5.10(a). The equivalent electrical model for Scott structure S1 including the metal segment and the contacts for entry and exit for the current into the structure is shown in Fig. 5.10(b). In this model,  $R_M$  is the resistance of the metal segment and  $R_P$  and  $R_{P1}$  are the resistance of the PCM segments in the structure. With  $L_i \gg l$ , there is no current flowing through

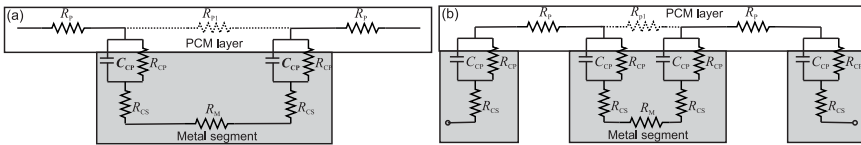


Figure 5.10: Electrical model of the metal to PCM interface (a) an individual metal segment (b) structure S1 with one metal segment.

the PCM resistance  $R_{P1}$ . Then by shifting the resistances and capacitances, a simplified equivalent network is derived for the structure as shown in Fig. 5.11.

In this model,  $R_S$  as the sum of all the series contact resistance ( $=\sum R_{CS}$ ),  $R_C$  as the sum of all the parallel capacitor resistance ( $=\sum R_{CP}$ ) and  $C_C$  is the effective capacitance of all the capacitors ( $=\sum C_{CP}$ ) in the structure. The total

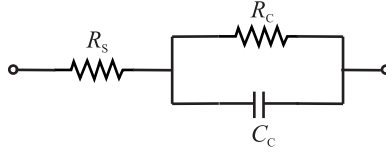


Figure 5.11: Equivalent electrical model for a TLM structure.

impedance of this model network in Fig 5.11,  $Z_M$  is calculated as:

$$Z_M = R_S + \left[ \frac{1}{\frac{1}{R_C} + j\omega C_C} \right] = R_S + \left[ \frac{R_C}{1 + j\omega R_C C_C} \right] \quad (5.1)$$

where the real and the imaginary parts is expressed as:

$$\text{Re}\{Z_M\} = R_S + \frac{R_C}{1 + (\omega R_C C_C)^2} \quad \& \quad \text{Im}\{Z_M\} = -\frac{\omega R_C^2 C_C}{1 + (\omega R_C C_C)^2} \quad (5.2)$$

The capacitance and resistance values of the structure are extracted by fitting the measured frequency dependence of  $Z_{CT}$  with the respective model equations  $Z_M$ . Fig. 5.12 shows the measured frequency dependence of real and imaginary part of  $Z_{CT}$  for Scott structure S1 in wafer-3, when fitted with eq. 5.4. The measured impedance values and the calculated fit show good agreement with the model.

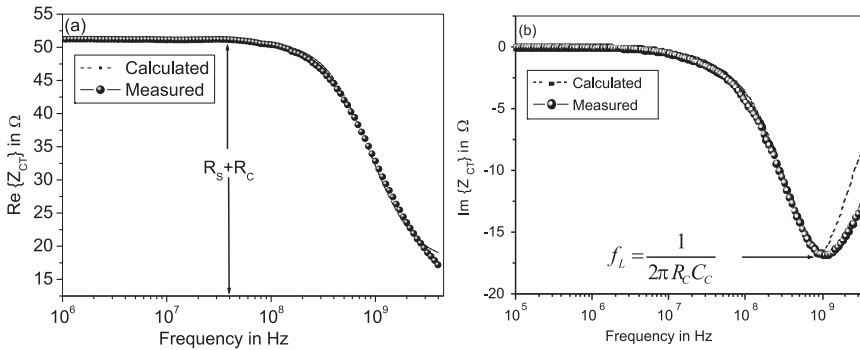


Figure 5.12: Change in  $Z_{CT}$  with frequency for structure S1 for wafer-3, with PCM width of  $20 \mu\text{m}$ . (a) Real part of  $Z_{CT}$ , (b) imaginary part of  $Z_{CT}$ . • represents the measured points and the line represents the calculated fit derived based on the electrical contact model.

The flat portion in Fig. 5.12(a), accounts for the sum total of all the resistance in the structure; that is  $R_S + R_C$ . If the total contact impedance of the structure ( $Z$ ) is plotted with frequency then in addition to  $R_S + R_C$ , the resistance of the metal  $R_M$  segment and PCM segment  $R_P$  in the structure is also included. At



higher frequencies,  $R_C$  will be shunted by the capacitor impedance lowering  $Z_{CT}$ . The rate of decrease of the impedance with frequency depends on  $C_C$  and  $R_C$ . The frequency at which the  $\text{Im}\{Z_{CT}\}$  in Fig. 5.12(b) reaches its minimum value is obtained by equating the first derivative of the imaginary part of the model equation to zero.

$$\frac{\partial(\text{Im}\{Z_M\})}{\partial\omega} = 0 \quad (5.3)$$

Thus obtained minimum frequency,  $f_L$  is:

$$f_L = \frac{1}{2\pi R_C C_C} \quad (5.4)$$

By fitting both these curves simultaneously the capacitor and resistor values in the contact model can be derived for all the Scott structures. From the fit an interface capacitance  $C_C$  of 5.4 pF, a parallel resistor  $R_C$  of 33.5  $\Omega$  and a series resistor  $R_S$  of 17.5  $\Omega$  are extracted for the metal segment in S1. The same calculation and fit for the same structure S1 in wafer 2 results in a  $C_C$  of 50 pF,  $R_C$  of 6.5  $\Omega$  and  $R_S$  of 18  $\Omega$  for the metal segment. For wafer-1, only a series resistor  $R_S$  of 1.9  $\Omega$  is extracted. In the case of wafer 3, the thicker oxidized interfacial layer results in a lower interfacial capacitance and a larger  $R_C$ . At higher frequency, the capacitive effect is negligible and it shunts  $R_C$ , hence only the series impedance will be visible. This is approximately the same for both wafer-2 and wafer-3 (See Fig. 5.7(a) and model).

The total capacitance value extracted from the different Scott structures for wafer-2 and wafer-3 are shown in Fig. 5.13. The extracted capacitance values from the measured impedance  $Z$  of the different structures (S1-S7) is shown in Fig. 5.13(a).  $Z$  includes the impedance of the contacts for entry and exit points for the current shown in the equivalent electrical model in Fig. 5.10(b). Hence the extracted value includes the capacitance contribution of these contacts in addition to the capacitance offered by the metal segments. Fig. 5.13(b) shows the extracted capacitance value from the total contact impedance  $Z_{CT}$ . The extracted value from  $Z_{CT}$  is the total capacitance contribution of only the metal segments in the structure.

As observed from Fig. 5.13(a), for both wafers the extracted capacitance is lower for S1, S2 and S3 as compared to the REF structure. Considering wafer-3, total capacitance extracted for the REF structure is 5.5 pF, which is 11 pF per contact interface. Now in the case of S1, with one metal segment, the total extracted capacitance of the structure is 2.3 pF. For this wafer, the transfer length ( $l=6.2 \mu\text{m}$ ) is smaller than the metal segment length ( $L_1=25 \mu\text{m}$ ), the current enters the metal at the leading edge and leaves the metal segment at the trailing contact edge, adding two metal to PCM contact interfaces in the current path. Thus, in the current path of Scott structure S1, four contact interfaces are present in series. This results in a capacitance of 9.2 pF per contact. The extracted capacitance value from  $Z_{CT}$  for S1 is 5.5 pF as shown in Fig. 5.13(b). For S2, having two metal segments ( $L_2=12.5 \mu\text{m}$ ), each of which adds two contact

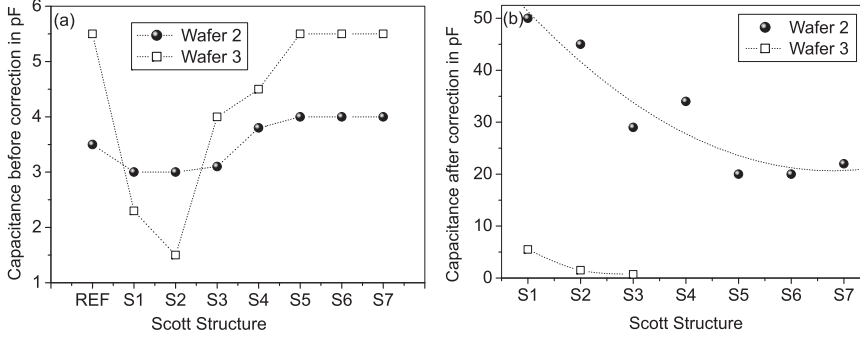


Figure 5.13: Extracted capacitance values for different Scott structures for wafer-2 and wafer-3. (a) From the total impedance of structure  $Z$ , (b) from the total contact impedance of only the metal segments  $Z_{CT}$ .

interfaces, six contact interfaces are present in series in the current path. The extracted capacitance value is 1.5 pF, which results in 9 pF per contact. In the case of other structures,  $l \gg L_i$  either the current is not completely entering the metal segment or, as is in the case of S5, S6, and S7, the current does not even enter the metal segment. In this case, only the capacitance contribution of the two contacts (as in the REF structure) is measured as seen in Fig. 5.13(a). A similar behaviour is observed for structures with a PCM width of 5  $\mu\text{m}$ . The interface capacitance depends on the area ( $A$ ) at the contact used for current transfer, which is determined by the  $W$  and  $l$ . Using this, the calculated capacitance density per contact for wafer-3 is approximately 8.8  $\mu\text{F}/\text{cm}^2$ .

For wafer-2,  $l$  and  $\rho_c$  are smaller and the interfacial layer is also thinner. Smaller  $l$  decrease the capacitance, while thinner interface increases the capacitance and at the same time increases the leakage.

### 5.3.4 Measurement limits

To validate the assumption in the previous section, that for structures with  $l \gg L_i$ , the metal segments are not in the current path, further analysis is performed on the Scott measurements. Furthermore, its influence on the measurements is also studied. Fig. 5.14 shows the plot of the measured  $\text{Im}\{Z\}$  of all Scott structures with frequency for all the three wafers. An identical behaviour which is independent of frequency is observed for all the structures in wafer-1. For structures in wafer-2 a frequency dependent behaviour is observed with a slight shift in  $f_L$ . In the case of wafer-3, identical frequency response is observed for REF structure and structures S5, S6 and S7. For this wafer from DC measurements, an  $l$  of 6.2  $\mu\text{m}$  is extracted.

To understand these measurements, the calculated  $Z_{CT}$  for structures in wafer-3 is plotted with frequency as shown in Fig. 5.15. The  $\text{Re}\{Z_{CT}\}$  for all the

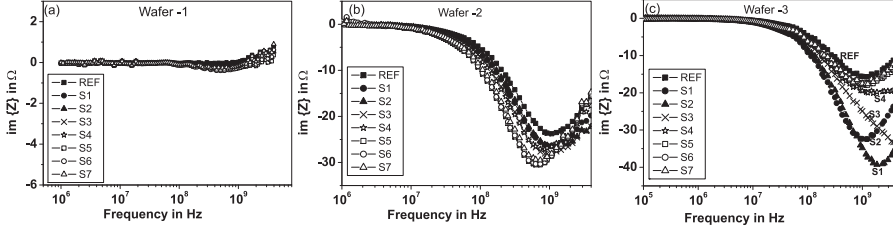


Figure 5.14: Frequency response plot of  $\text{Im}\{Z\}$  of the Scott structures with frequency for all three wafers.

structures is normalised to the same point at the start of the frequency sweep. Frequency dependence in this measurement range is observed only for structures S1, S2 and S3. For all other structures  $l$  is larger  $L_i$ . Hence the current doesn't enter the metal segments and hence does not make any capacitance contribution. For these structures, the frequency response is identical to that of the REF structure as seen from Fig. 5.14. The frequency response of  $Z_{CT}$  depends on  $R_C$  and  $C_C$ . In Scott structures where current enters the metal, the resistance

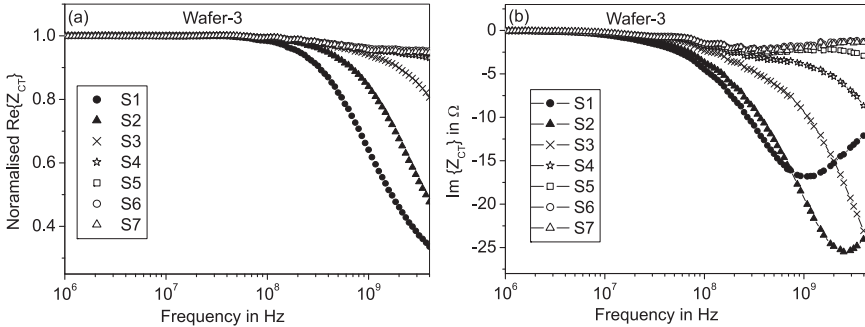


Figure 5.15: The real and imaginary part of the  $Z_{CT}$  with frequency for the wafer-3.

of the PCM in that part is shorted by the metal and at the same time adds two contact resistances. For structures with  $l < L_i$ ,  $Z_{CT}$  increases from the reference value due to the addition of contact impedances every time the current enters and leaves the metal segments. For structures with  $l \gg L_i$ , the current will not enter the metal segment and is passed through the PCM layer above it. In this case, the resistance of the PCM layer  $R_{P1}$  is added to the reference value, the value of which is the maximum measured for the Scott structures. The calculated differential  $Z_{CT}$ , at 100 MHz and at 4 GHz for all the three wafers is plotted as is in Fig. 5.16. Differential  $Z_{CT}$  is calculated using eq. 2.20 and hence should be zero for the REF structure for all the wafers.

As observed from Fig. 5.16(a), differential  $Z_{CT}$  measured at 100 MHz (same

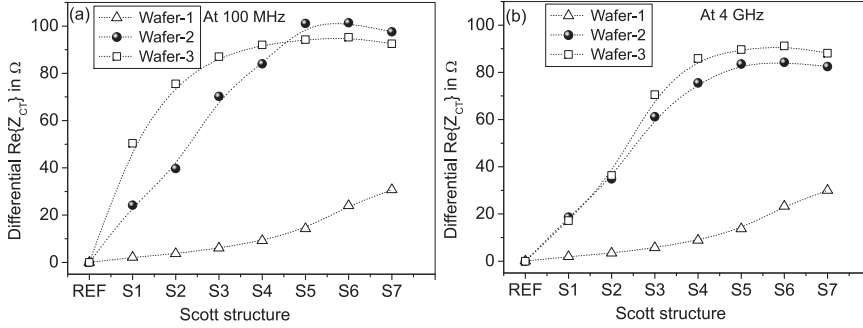


Figure 5.16: Change in  $Z_{CT}$  of the Scott structures for all the three wafers. (a) at 100 MHz, (b) at 4 GHz.

as DC measurements) saturates at around 90  $\Omega$  for wafer-2 from S5 (with  $L_i=1.59 \mu\text{m}$ ,  $l=3.2 \mu\text{m}$ ) and for wafer-3 from S4 (with  $L_i=3.15 \mu\text{m}$ ,  $l=6.2 \mu\text{m}$ ) onwards. The PCM  $R_{SH}$  measured in all three wafers is approximately 70  $\Omega/\square$ . The width of the PCM layer in the structures is 20  $\mu\text{m}$ . Due to the geometry of the structures the metal segments account for 1.25 squares for a maximum increase in resistance of approximately 90  $\Omega$ . At 4 GHz, wafer-2 and wafer-3 reach approximately the same  $\rho_c$ , and hence they follow almost the same curve as seen in Fig. 5.16 (b). For wafer-1, differential  $Z_{CT}$  did not saturate for both frequencies. The slight differences in the saturated differential  $Z_{CT}$  value for wafer 2 and wafer 3 are due to the differences in PCM  $R_{SH}$  in both the wafers. As observed from Fig. 5.8 for wafer-3,  $\text{Re}\{Z_C\}$  decreases at higher frequencies for structures with  $L_i$  larger than  $l$ . That is only for structures S1, S2 and S3.

The exchange of the current at the metal to PCM interface for metal segments of different length  $L_i$  can be further understood by studying the fraction of current in the metal segment. Based on the model in eq. 2.25 the fraction of the current in the metal ( $I(x)/I$ ) as a function of the distance  $x$  calculated for all three wafers for S1 ( $L_i=25 \mu\text{m}$ ), S4 ( $L_i=3.15 \mu\text{m}$ ) and S7 ( $L_i=0.36 \mu\text{m}$ ) is shown in Fig. 5.17.

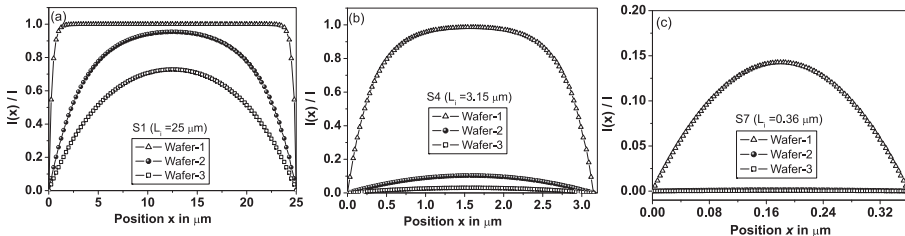


Figure 5.17: Fraction of the current in the metal segments ( $L_i=25 \mu\text{m}$ ,  $3.15 \mu\text{m}$ , and  $0.36 \mu\text{m}$ ) as a function of position  $x$  for all the three wafers.

For wafer-1, the current completely enters and leaves the 25  $\mu\text{m}$  metal segment and the 3.15  $\mu\text{m}$  segment. For the 0.36  $\mu\text{m}$  metal segment, the current does not have enough length to enter the metal segment completely, and hence only 15% enters the metal segment and the remaining 85% remains in the PCM segment. For wafer-2, for the 25  $\mu\text{m}$  metal segment almost all the current enters the segment, but only 10% of the current enters for the 3.16  $\mu\text{m}$  segment and no current enters for the 0.36  $\mu\text{m}$  segment. In the case of wafer-3, only 70% of the current enters the 25  $\mu\text{m}$  metal segment and no current enters the other two smaller segments.

## 5.4 Linear-TLM measurements

In this section, the HF measurements performed on linear TLM structures modified in the GSG configuration are presented. As compared to Scott TLM structures, these structures have a fixed contact area for all the structures, but with different spacing  $d$  between the contacts. Structures were available with a  $d$  of 50  $\mu\text{m}$ , 20  $\mu\text{m}$ , 10  $\mu\text{m}$ , 5  $\mu\text{m}$ , 2  $\mu\text{m}$  and 1  $\mu\text{m}$  all having the same contact length  $L_C$  of 10  $\mu\text{m}$ . The width of the PCM layers available are 50  $\mu\text{m}$ , 20  $\mu\text{m}$ , 10  $\mu\text{m}$ , 5  $\mu\text{m}$ , 2  $\mu\text{m}$ , and 1  $\mu\text{m}$ . The SEM image of an individual linear TLM structure is shown in Fig. 5.20. From the DC measurements performed on these structures, a  $\rho_c$  of  $6.8 \times 10^{-7} \Omega\cdot\text{cm}^2$  was extracted for wafer-1 and  $5.6 \times 10^{-5} \Omega\cdot\text{cm}^2$  for wafer-3.

From the S-parameter measurements performed on GSG test structures, the real and the imaginary part of the differential impedance  $Z$  offered by each structure is calculated using eq. 2.26. These measurements for wafer-1 and wafer-3 show identical frequency response behaviour as shown in Fig. 5.7. The  $\text{Re}\{Z\}$  plotted with  $d$  measured for different frequencies in the range from DC to 4 GHz is shown in Fig. 5.18. For both the wafers, a linear TLM like behaviour with

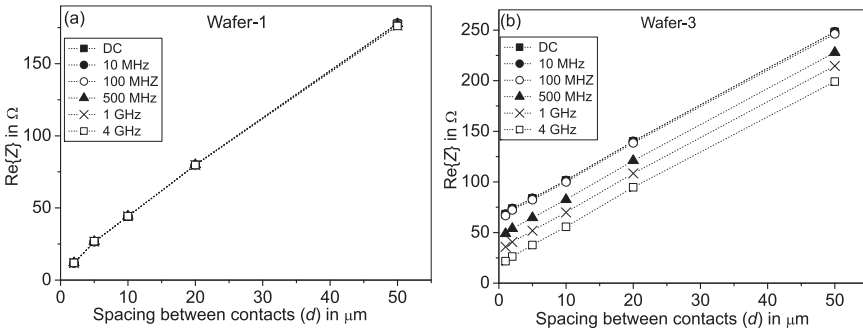


Figure 5.18:  $\text{Re}\{Z\}$  with the spacing between contacts,  $d$  for wafer-1(a) and wafer-3(b).

$\text{Re}\{Z\}$  increasing with  $d$  is observed. For wafer-1, the  $\text{Re}\{Z\}$  is independent

of the frequency while for wafer-3,  $\text{Re}\{Z\}$  decreases with increase in frequency. From this curve, the  $R_{\text{SH}}$ ,  $l$  and  $\rho_c$  can be extracted as explained in Chapter 2.3.  $R_{\text{SH}}$  calculated from the slope of the curve remains constant at approximately  $70 \Omega/\square$  for both the wafers and for all the frequencies studied. This indicated that the sheet resistance of PCM in the crystalline state is independent of frequency up to 4 GHz. The extracted  $\rho_c$  with frequency for both the wafers is shown in the Fig.5.19.

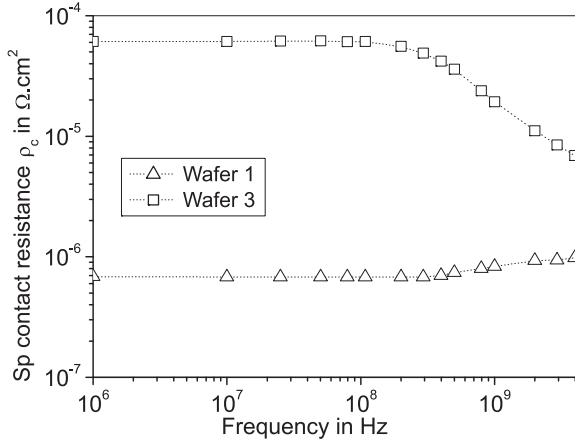


Figure 5.19:  $\rho_c$  with measurement frequency for wafer-1 and wafer-3.

For wafer-1, the extracted  $\rho_c$  is almost independent of frequency, while for wafer-3,  $\rho_c$  value decreases with frequency due to the presence of an oxidized capacitive interface. It should be noted that, a higher  $\rho_c$  value is extracted for wafer-1 from linear TLM structure compared to Scott TLM structures. This  $\rho_c$  value is the measurement limit for linear TLM structures [137] and hence a reliable result is not obtained. Scott TLM structures are reported to be suitable in this range of  $\rho_c$  values [138]. The frequency dependence of contact impedance for these structures can be electrically modelled with the same resistance-capacitance network shown in Fig. 5.9. The complete electrical model superimposed on the SEM image of a linear TLM structure is shown in Fig. 5.20. where,  $R_P$  is the resistance of the PCM line. Shifting the resistances and capacitances, a simplified equivalent network shown in Fig. 5.11 is derived with:

$$R_S = 2R_{CS} + R_P; \quad C_C = C_{CP}/2; \quad R_C = 2R_{CP} \quad (5.5)$$

The  $\text{Re}\{Z\}$  and  $\text{Im}\{Z\}$  with frequency for TLM structure with  $W$  of  $20 \mu\text{m}$  and  $d$  of  $20 \mu\text{m}$  in wafer-3 is shown in Fig. 5.21. The measured  $Z$  and the calculated fit using model eq. 5.3 shows good agreement. From this fit,  $R_C$  of  $43 \Omega$ ,  $C_C$  of  $6.5 \text{ pF}$  and  $R_S$  of  $97 \Omega$  are extracted for this structure. Similar measurements were performed on all the structures with different spacing between the contacts.

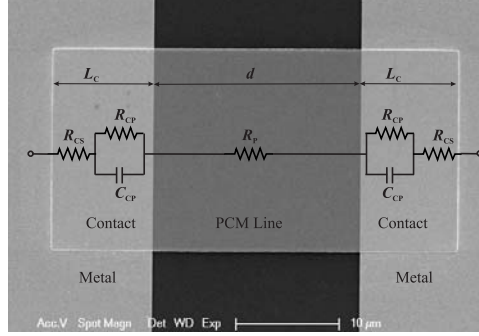


Figure 5.20: Electrical model of a linear TLM structure superimposed in its SEM image.

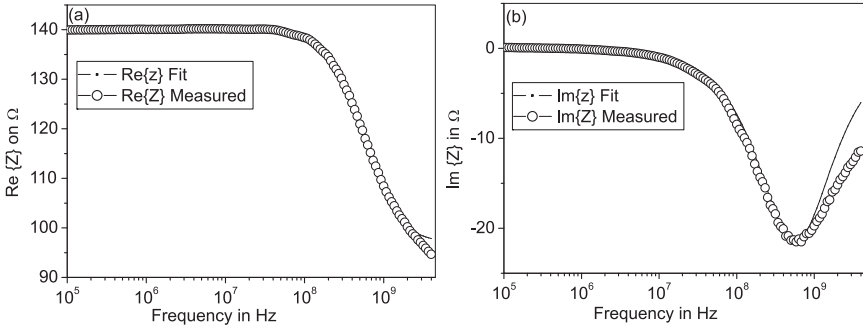


Figure 5.21: Change in (a)  $\text{Re}\{Z\}$  and (b)  $\text{Im}\{Z\}$  with frequency for linear TLM structure.  $\circ$  represents the measured points and the line represents the derived fit.

$C_{CP}$  and  $R_{CP}$  were then calculated using eq. 5.6, which remains the same for all the structures. The extracted  $R_S$  includes  $R_P$  and  $R_{CS}$ , and hence increases with  $d$  the equation of which could be rewritten as:

$$R_S = 2R_{CS} + R_P = 2R_{CS} + \frac{R_{SH}d}{W} \quad (5.6)$$

A linear relationship is observed for  $R_S$  with  $d$  as evident from Fig. 5.22. The value of  $R_{CS}$  is then calculated from the intercept of the curve at  $d = 0$ . From the slope of the curve  $R_{SH}$  can also be calculated.

The summary of the extracted contact parameters from HF linear TLM measurements for TiW to crystalline doped-Sb<sub>2</sub>Te contacts for all three wafers with different interface treatment is listed in Table 5.2.

The extracted capacitance per contact for wafer-3, from linear TLM structures with contact area ( $A = W \times L_C$ ) of  $20 \mu\text{m} \times 10 \mu\text{m}$  is 12.5 pF and from Scott TLM (REF structure) of  $20 \mu\text{m} \times 35 \mu\text{m}$  is 11 pF. The almost identical extracted  $C_{CP}$  values indicate that its value is determined by the transfer length at the contact.

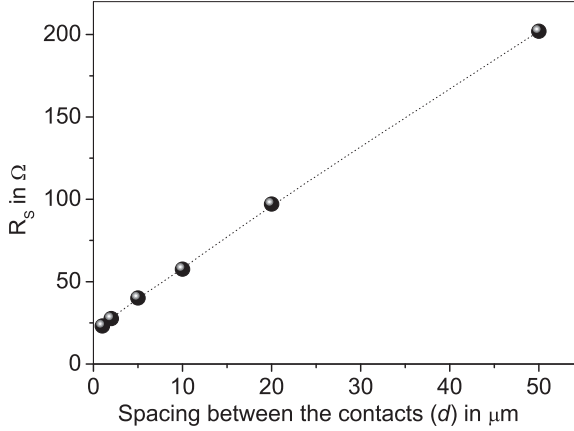


Figure 5.22: Calculated  $R_s$  with  $d$  of the TLM structure.  $W=20 \mu\text{m}$ .

Table 5.2: Summary of extracted TiW to PCM contact parameters for all the three wafers

PCM width	Wafer 1		Wafer 2		Wafer 3	
	20 $\mu\text{m}$	5 $\mu\text{m}$	20 $\mu\text{m}$	5 $\mu\text{m}$	20 $\mu\text{m}$	5 $\mu\text{m}$
$R_{CP}$ in $\Omega$	N.A	N.A	41.3 $\pm$ 13	227 $\pm$ 57	22.3 $\pm$ 0.6	110 $\pm$ 14
$C_{CP}$ in pF	N.A	N.A	6.8 $\pm$ 0.49	1.6 $\pm$ 0.05	12.5 $\pm$ 0.45	2.5 $\pm$ 0.15
$R_{CS}$ in $\Omega$	4.4	13.8	6.65	35	10.5	44.3
$R_{SH}$ in $\Omega/\square$	68	72	76.4	73.5	72.8	78.5
$f_L$ in MHz	N.A	N.A	567	438	570	562

## 5.5 Summary and conclusions

In this chapter, test structures and a data extraction procedure are presented that is suitable for electrical contact interface characterization at high frequency. This method can separate the interface capacitance from the interface resistance values. Scott TLM and linear TLM structures have been modified in the GSG configuration to perform contact resistance measurements as a function of frequency. These test structures have been fabricated with three different interface treatments (Ar pre-clean, oxygen plasma) resulting in different metal to PCM contact resistance values. From the DC measurements; for Scott TLM structures, a  $\rho_c$  value of  $8 \times 10^{-8} \Omega.\text{cm}^2$  for wafer-1,  $8.6 \times 10^{-6} \Omega.\text{cm}^2$  for wafer-2 and  $3.2 \times 10^{-5} \Omega.\text{cm}^2$  for wafer-3 is extracted, while measurements on the linear TLM structure results in a  $\rho_c$  value of  $6.8 \times 10^{-7} \Omega.\text{cm}^2$  for wafer-1 and  $5.6 \times 10^{-5} \Omega.\text{cm}^2$  for wafer-3. The measurement limitations of linear TLM in the lower  $\rho_c$  range resulted in the higher extracted values for wafer-1 from these structures. For the



same reason, a reliable  $\rho_c$  is not obtained for wafer-2. Detailed comparison and measurement limits of both the structure is given in Chapter 2.5

Two port S-parameter measurements were performed on Scott TLM and linear TLM test structures with frequencies up to 4 GHz. From the measured S-parameters, the contact impedance and  $\rho_c$  values are calculated with signal frequency.  $\rho_c$  values extracted from the GSG structures at low frequencies correspond to the values obtained from identical test structures measured at DC in the four point force-sense configuration. In case of structures with higher contact resistance (wafer-2 and wafer-3), a frequency dependence is observed for contact impedance. This is attributed to the presence of the interfacial layer at the contact that acts like a capacitor. The metal to PCM interface is electrically modeled with a resistance in series with a parallel combination of capacitor and resistor. Comparing the frequency response of the measured contact impedances with the electrical model, the different resistor and capacitor values are extracted.

Compared to linear-TLM structures, Scott-TLM structures are better suited for high frequency measurements, since more parameters could be extracted from these structures. A linear-TLM structure has contacts with a fixed area resulting in the same extracted interfacial capacitance value for all the structures. For Scott-TLM structures, the extracted capacitance value changes for each structure due to the change in contact area. Impedance matching is also easily possible for Scott-TLM structures by adjusting the geometry of the structure. This is essential to increase the accuracy of extracted parameters from high frequency measurements. At HF the effective contact resistance is lower for poor interfaces. The series interfacial capacitor formed has lower impedance at higher frequencies. For a PCRAM cell that is operated at high frequencies, the effective contact resistance is lower and consequently it is less sensitive to the processing of the contacts.



## Influence of parasitic current paths on resistance measurements

*Accurate electrical characterization of test structures and devices requires identification and correction for parasitic current paths in the measurement network. Sidewalls formed during etching of thin film phase change material layers in argon plasma can result in parasitic current paths in the structures. In the first part of this chapter thin film structures with re-deposited sidewalls are realized and they are experimentally characterized by electrical resistance measurements on Van der Pauw test structures. The impact of conducting sidewalls on contact resistance measurements and data extraction from cross bridge Kelvin resistor structures is discussed. The error introduced in the electrical resistance measurements from these test structures is analytically modeled. In the attempt to characterize the crystalline PCM to amorphous PCM contacts, a non-uniform interface is formed due to partial crystallization of PCM. This non-uniform contact interface also results in the formation of parasitic current paths which influence the contact resistance measurements from these structures. The details of the test structures used and measurement procedures are described in the second part of this chapter. The experimental results are substantiated with TEM analysis of these structures.*

## 6.1 Thin-film structures with re-deposited sidewalls

Thin film PCM layers are patterned by Reactive Ion Etching (RIE) with a protective mask. RIE, which is a combination of physical sputtering and chemical etching in a plasma, is the preferred etching process for achieving anisotropic etch profiles. The high etch rate of PCM (doped-Sb<sub>2</sub>Te and Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub>) towards commonly used etch chemistries results in large (isotropic) under-etching [139]. With the inclusion of argon in the etch chemistry, physical ion bombardment becomes a dominant factor for PCM etching [140]. Sputter etching due to ion bombardment in argon plasma limits the under-etching of the PCM layers. However in the case when sputtering dominates the etch rate, fences or sidewalls of the re-deposited material can be formed either by direct re-deposition onto the masking layer or by condensation from the gas phase [141]. The sidewalls formed by direct re-deposition on the protective resist mask during etching of the PCM layers in argon plasma is schematically shown in Fig. 6.1(a). These sidewalls may split and standup or fall over locally with or without breaking (electrical) connections. Standing and fallen sidewalls formed after mask removal are shown in Fig. 6.1(b). In this section, the presence of sidewalls in a thin film device and

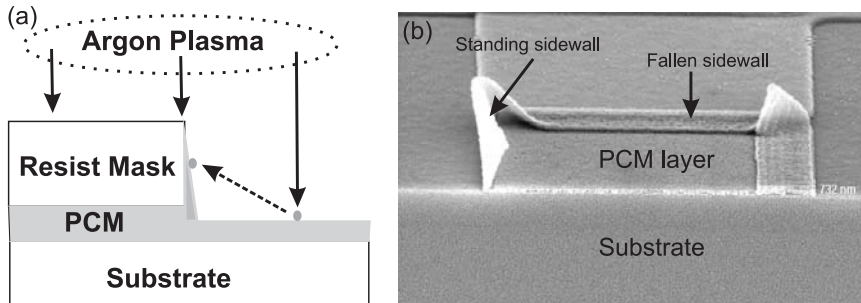


Figure 6.1: Schematic representation showing the re-deposition of the PCM layer on to the resist sidewall during etching. (b) SEM image of standing and fallen sidewall formed around a PCM layer after etching and mask removal.

its impact on the electrical characterization and data extraction from Van der Pauw and CBKR structures is investigated. The nature of the sidewalls formed (standing or fallen) is correlated by SEM inspection to the errors introduced in the measurements and data extraction from these structures.

### Measurement structures

Thin-film TiW and PCM Van der Pauw structures (Fig. 2.12) and TiW to PCM CBKR structures (Fig. 2.3) were fabricated on oxidized silicon wafers.

First, a 50 nm TiW metal layer is deposited by sputtering and is patterned to form the metal van der Pauw structure and the bottom electrode layer of the CBKR structure. Then, a 50 nm PECVD SiO<sub>2</sub> is deposited at 400 °C through which electrical contacts are defined between TiW and the subsequent deposited PCM layer. The PCM layer is deposited by sputtering and is patterned to form the Van der Pauw structures and the top layer of the CBKR structure. Both TiW and PCM layers are patterned by plasma etching using a 800 nm thick photo-resist mask. TiW layers are patterned in a chlorine-based chemistry. The chemical nature of this etching resulted in volatile components and hence no sidewall formation. Due to the high chemical reactivity of PCM, it is etched in argon rich plasma, which in this case led to formation of sidewalls due to direct re-deposition. After patterning of the layers, the resist mask is removed in oxygen plasma. The sidewall formed around the PCM layer in the CBKR structure is shown in Fig. 6.2.

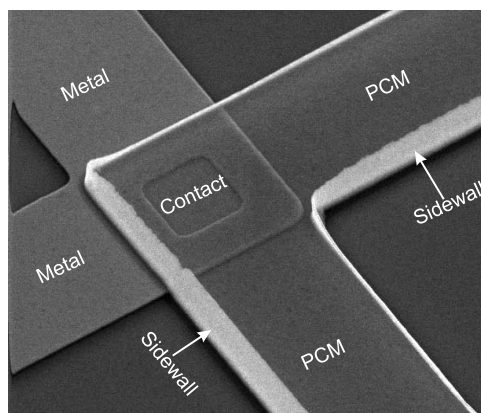


Figure 6.2: SEM image of standing sidewalls formed around the PCM layer after etching in the CBKR structure.

### 6.1.1 Van der Pauw resistance measurements

Sheet resistance measurements were performed on Van der Pauw structures to detect the presence of sidewalls and to characterize the error introduced in the calculation of resistivity from these structures with sidewalls. These measurements were performed on square structures with different edge length,  $S$  of 2  $\mu\text{m}$ , 5  $\mu\text{m}$ , 10  $\mu\text{m}$ , 20  $\mu\text{m}$  and 50  $\mu\text{m}$ . From these measurements, the resistivity of the layer is calculated using eq. 2.28. The measured PCM resistivity with  $S$  is shown in Fig. 6.3. These measurements are for PCM structures with standing and fallen sidewalls and for TiW structures with no sidewalls. The calculated resistivity for the TiW layer is almost independent of the dimensions of the Van der

Pauw structures. Only for the smallest structure ( $S = 2 \mu\text{m}$ ), a lower value is observed. This is due to non-ideal peripheral contacts with contact length of  $1 \mu\text{m}$ , which is more than 10% of  $S$ . Then, for the calculation of  $R_{\text{SH}}$  from square Van der Pauw structures, a correction is required for the geometrical factor  $\pi/\ln(2)$  [44]. In the case of PCM structures with standing sidewalls observed from SEM, the measured resistance increases with decreasing  $S$ . In the case of Van der Pauw structures with fallen sidewalls, the calculated resistivity of the layer is lower than that without sidewalls.

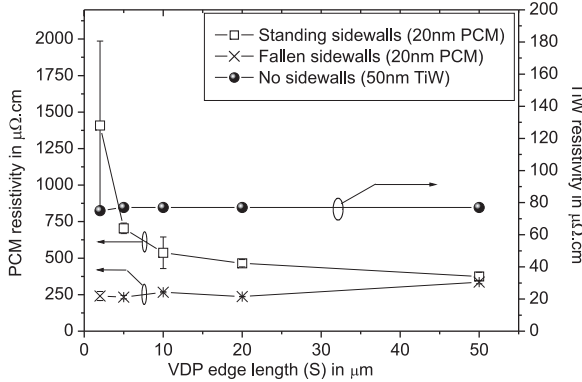


Figure 6.3: Resistivity with  $S$  calculated for PCM structures with standing and fallen sidewalls compared to TiW without sidewalls.

Sidewalls are formed by direct re-deposition onto the vertical edge faces of the masking layer. Hence the height of sidewalls is mainly determined by the thickness of the resist mask, which is approximately  $1 \mu\text{m}$ . The sidewall material could have a lower density and so a higher resistivity than the layer itself. By first order approximation, the formation of standing sidewalls expands the Van der Pauw square equally on all the sides. The resulting final structure will also be a square but the expanded sidewall region will have a larger resistivity. In addition, expansion of the Van der Pauw square due to the formation of standing sidewalls moves the position of the electrical contacts from the corners to the inside. As opposed to the case of having point contacts at the corners of the square, if they are moved inside, the geometrical factor used in the calculation of  $R_{\text{SH}}$  changes. The relative error introduced in the sheet resistance due to the placement of contacts inside by a distance  $d$  for a circular structure of diameter  $D$  is given by [66]:

$$\frac{\Delta R_{\text{SH}}}{R_{\text{SH}}} = \frac{d^2}{2D^2 \ln 2} \quad (6.1)$$

For smaller van der Pauw structures, the relative contribution of sheet resistance of sidewalls and the effect of placement of the contacts inside the square is

larger. This explains the increase in resistivity and larger spread in the measurements for smaller van der Pauw structures with standing sidewalls as shown in Fig. 6.3. In the case of PCM structures with sidewalls fallen onto the layer itself, the thickness of the PCM layer is increased locally around the edges. An increase in the thickness of the layer results in lower  $R_{SH}$  (using eq. 2.28) as seen in Fig. 6.3. The effect of the side walls is larger for smaller structures since the relative area over which the side walls will be fallen is larger for these structures.

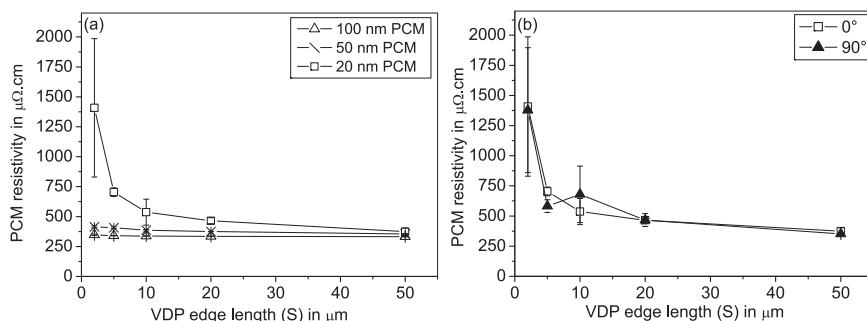


Figure 6.4: (a) PCM resistivity with  $S$  for 20 nm, 50 nm and 100 nm PCM layers having side walls (b) structure with 20 nm thick PCM layer having standing sidewalls measured in two different current directions. The error bar indicates the spread in measurements at each point.

The relative error introduced in the calculated resistivity by moving the contacts inside is independent of the thickness and  $R_{SH}$  of the layer (eq. 6.1). The PCM resistivity with  $S$  for three different layer thicknesses is shown in Fig. 6.4(a). The resistivity deviates more in the case of thinner PCM layers as compared to thicker layers. Hence for the thinner layer, a larger contribution of the sidewalls is observed. To examine the symmetry of van der Pauw structures with sidewalls, measurements were performed by rotating the current force and the voltage measurement terminals by 90 degrees four times. Fig. 6.4(b) shows the PCM resistivity measured in two different directions. Measurements in opposite directions rotating the terminals by 180 degrees results in the same electrical resistance.

In practice, the sidewalls do not exhibit a regular shape or uniform resistivity by nature of its formation. They may split, stand up or fall over locally with or without breaking (electrical) connections. This means that, due to these inhomogeneities, the structure can become electrically asymmetric as seen in Fig. 6.4(b). This will be more pronounced for the smaller structures and it also results in a larger spread in measurements. Electrical resistance measurements on Van der Pauw structures, with a wide range of dimensions can be used as an indicator for the presence of sidewalls. When the height of sidewalls in these structures is in the same order as the dimensions of the structure, the measured resistance values deviate more from its ideal value.

### 6.1.2 CBKR contact resistance measurements

The effect of PCM sidewalls on the extracted  $\rho_c$  is demonstrated using contact resistance measurements on CBKR structures. The measured resistance ( $R_K$ ) with  $\delta$  for CBKR structures with standing sidewalls around the PCM layer (see Fig. 6.2) is shown in Fig. 6.5(a). These measurements are for structures with the TiW to PCM contact area,  $A$  of  $9 \mu\text{m}^2$ . The  $\rho_c$  extracted for each measurement point using eq. 2.10 is shown in Fig. 6.5(b). The measured  $R_K$  includes, contact

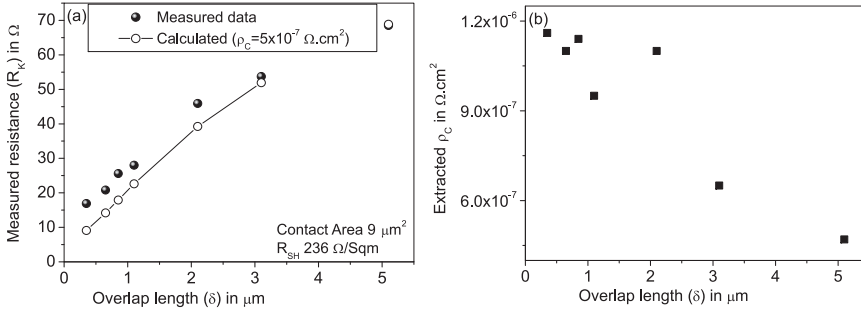


Figure 6.5: (a)  $R_K$  with  $\delta$  for CBKR structures with standing sidewalls.  $\bullet$  shows measurement points and  $\circ$  shows the values calculated with  $\rho_c$  extracted for  $\delta = 5 \mu\text{m}$ . (b) Extracted  $\rho_c$  with  $\delta$  for measurement points in Fig. 5.5(a).

resistance  $R_C$  and the contribution of overlap  $R_D$ , which is dependent on PCM  $R_{SH}$  and the  $\delta$  (see eq. 2.10).  $\rho_c$  is a property of the interface and should be independent on the  $\delta$  around the contact. In Fig. 6.5(b) the extracted  $\rho_c$  decreases with  $\delta$  for structures with standing PCM sidewalls. The extracted  $\rho_c$  for  $\delta$  of  $0.35 \mu\text{m}$  is  $1.1 \times 10^{-6} \Omega \cdot \text{cm}^2$  and for  $\delta$  of  $5 \mu\text{m}$  is  $5 \times 10^{-7} \Omega \cdot \text{cm}^2$ . The formation of standing sidewalls expands the  $\delta$  by its height, which directly influences  $R_D$  and  $R_K$ . This results in an inaccurate extraction of  $\rho_c$  from these CBKR structures. The effect of the sidewalls will be relatively smaller for structure with the largest  $\delta$  and the obtained  $\rho_c$  for which approximates almost the actual value. The largest  $\delta$  available is  $5 \mu\text{m}$  and the extracted  $\rho_c$  from this structure is  $5 \times 10^{-7} \Omega \cdot \text{cm}^2$ . Using eq. 2.10, the  $R_K$  values are calculated with a  $\rho_c$  of  $5 \times 10^{-7} \Omega \cdot \text{cm}^2$  and PCM  $R_{SH}$  of  $236 \Omega/\square$  (from Van der Pauw structures) is shown in Fig. 6.5(a). With standing sidewalls, the largest deviation in measured  $R_K$  values is observed for smallest  $\delta$ . In this case,  $R_K$  values for structures with the smallest delta ( $\delta$  of  $0.35 \mu\text{m}$ ) are over-estimated by approximately 50% and the extracted  $\rho_c$  by more than 60% of the actual values.

Sidewalls can also be formed irregularly in the CBKR structures. Fig. 6.6 shows SEM images of three structures with the same contact area of  $4 \mu\text{m}^2$  but with different  $\delta$ . The CBKR structure; in Fig. 6.6(a) has a  $\delta$  of  $0.35 \mu\text{m}$  with irregular sidewalls formed around the PCM layer, in Fig. 6.6(b) has a  $\delta$  of  $0.65 \mu\text{m}$  without sidewalls, and in Fig. 6.6(c) has a  $\delta$  of  $1.1 \mu\text{m}$  with PCM sidewalls



formed on one side of the structure. The measured resistance  $R_K$  with  $\delta$  for these

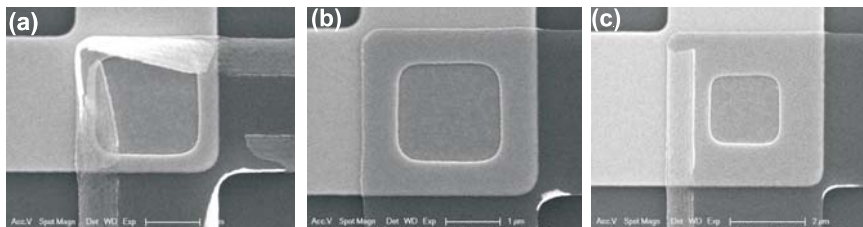


Figure 6.6: SEM images of CBKR structures showing different pattern of sidewall formation. All structures have the same contact area of  $4 \mu\text{m}^2$  but different  $\delta$  (a)  $\delta$  of  $0.35 \mu\text{m}$  with irregularly formed PCM sidewalls on all sides, (b)  $\delta$  of  $0.65 \mu\text{m}$  with no PCM sidewalls, (c)  $\delta$  of  $1.1 \mu\text{m}$  with PCM sidewalls formed only on one side.

structures is shown in Fig. 6.7(a). The  $\rho_c$  extracted from these measurements is shown in Fig. 6.7(b). The  $\rho_c$  extracted for structures without sidewalls (in

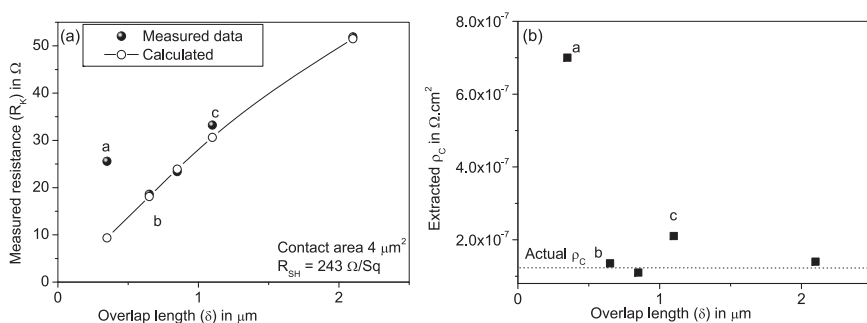


Figure 6.7: (a)  $R_K$  with  $\delta$  for CBKR structures with irregularly formed sidewalls. The inset characters a, b and c corresponds to the SEM image in Fig. 6.  $\bullet$  shows the measurement points and  $\circ$  shows the calculated value minimizing the effect of sidewalls. (b) Extracted  $\rho_c$  with  $\delta$  for CBKR structures. The dotted line represents the actual  $\rho_c$  for this contact.

Fig 6.6(b)) is  $1.1 \times 10^{-7} \Omega.\text{cm}^2$ . The calculated  $R_K$  values using eq. 2.10 with this  $\rho_c$  value and PCM  $R_{\text{SH}}$  of  $243 \Omega/\square$  is shown in Fig. 6.7(a). The calculated  $R_K$  coincides with the measurement points for structures without sidewalls. The extracted  $\rho_c$  is higher for measurement points a and c, which are associated to the CBKR structures for which sidewalls are observed from the SEM image (Fig. 6.6(a) and Fig 6.6(c) respectively). Also in this case, the deviation in  $\rho_c$  with sidewalls is larger for structure with smaller  $\delta$ .

According to eq. 2.10,  $R_K$  depends on PCM  $R_{\text{SH}}$ . To investigate the effect of sidewalls with PCM  $R_{\text{SH}}$ , additional measurements were performed on TiW to  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  structures fabricated with a thermal budget of  $120 \text{ }^\circ\text{C}$ . The

measured  $R_K$  with  $\delta$  for  $A$  of  $4 \mu\text{m}^2$  is shown in Fig. 6.8(a). The inset shows the measurements on structures with contact area of  $1 \mu\text{m}^2$ ,  $4 \mu\text{m}^2$ ,  $9 \mu\text{m}^2$ ,  $16 \mu\text{m}^2$ . From these measurements, the average  $\rho_c$  of  $3.9 \times 10^{-6} \Omega.\text{cm}^2$  is extracted. The accompanying Van der Pauw structures measure a PCM resistivity of  $12.2 \text{ m}\Omega.\text{cm}$ . As observed from Fig. 3.1,  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  in these structures is in meta-stable state. When annealed at a temperature of  $250 \text{ }^\circ\text{C}$  for 5 min in  $\text{N}_2$  ambient, the resistivity of PCM in these structures lowers to  $416 \mu\Omega.\text{cm}$ . The  $R_K$  with  $\delta$  measurements for the same structures after  $250 \text{ }^\circ\text{C}$  anneal is shown in Fig. 6.8(b). The  $\rho_c$  extracted from these measurements is approximately  $1.7 \times 10^{-6} \Omega.\text{cm}^2$ . The influence of side walls on  $R_K$  values is more pronounced for CBKR structures

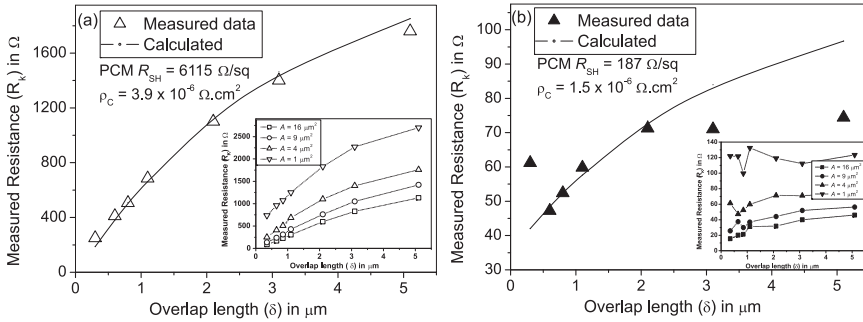


Figure 6.8:  $R_K$  with  $\delta$  for CBKR structures with contact area ( $A$ ) of  $1 \mu\text{m}^2$ ,  $4 \mu\text{m}^2$ ,  $9 \mu\text{m}^2$  and  $16 \mu\text{m}^2$ .(a) before anneal; (b) After  $250 \text{ }^\circ\text{C}$  anneal. The inset values show the PCM resistivity and extracted  $\rho_c$ .

with lower  $R_{SH}$  values. This is ascribed to the more pronounced current spreading paths formed.

In this section, the presence of re-deposited sidewalls and its influences on resistance measurements from Van der Pauw structures and from CBKR structures were investigated. However, the formation of re-deposited sidewalls in PCM devices can be minimized. At the same time an almost uniform profile can be fabricated by optimization of the etch gas mixing ratio, tuning the process parameters [140][142][143] or by the use of a hard mask [139]. In the following section, PCM layers have been etched in an optimized Ar/Cl environment to minimize re-deposited residues.

## 6.2 Amorphous PCM to crystalline PCM contact resistance

In the reset state of the PCRAM cell, a part of the PCM in the cell is in the amorphous state. The top view TEM image of a PCRAM line cell in the reset state with metal electrodes and regions of crystalline PCM and amorphous

PCM is shown in Fig. 6.1(a). On the macroscopic scale, two different types of interfaces exist in this cell: the metal electrode to crystalline PCM interface and the crystalline PCM to amorphous PCM interface. The presence of the latter

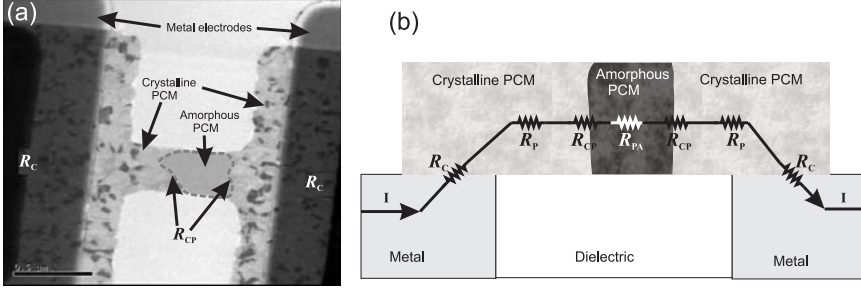


Figure 6.9: PCRAM line cell in the reset state showing the metal electrode and the amorphous and crystalline PCM regions. (a) Top view TEM image (b) Schematic cross-section with the equivalent electrical network.

offers an additional resistance to the flow of current. Two metal to PCM contact resistance ( $2 \times R_C$ ) and two crystalline PCM (c-PCM) to amorphous PCM (a-PCM) contact resistance ( $2 \times R_{CP}$ ) exist in the current path of the cell. The schematic cross-section of the cell is shown in Fig. 6.9(b). The total resistance of the cell in the reset state  $R_{\text{reset}}$ , including the c-PCM resistance  $R_P$  and the a-PCM resistance  $R_{PA}$  is represented as:

$$R_{\text{reset}} = 2R_C + 2R_P + 2R_{CP} + R_{PA} \quad (6.2)$$

The resistance of interconnect metal  $R_M$  is neglected. The value of  $R_C$  and  $\rho_c$  for different CMOS compatible metal electrodes to PCM are given in chapter 4. The aim of this section is to determine  $R_{CP}$  and express it in terms of a-PCM to c-PCM specific contact resistance  $\rho_{CP}$ . The test structures, the fabrication steps and the electrical measurements are presented here.

## Measurement structures

Kelvin resistor and TLM structures were fabricated to characterize the c-PCM to a-PCM interfacial resistance. To fabricate these structures, first a metal layer (500 nm Al or 100 nm TiW) is sputter deposited on a clean oxidized silicon wafer and is patterned to form the bond pads to facilitate electrical probing. Subsequently, a 50 nm amorphous doped-Sb<sub>2</sub>Te layer is sputter deposited and is crystallized by annealing at 200 °C for 5 min in N<sub>2</sub> ambient. This crystalline PCM layer is patterned in Ar-Cl plasma to form the bottom electrode layer (bottom PCM layer). A second 50 nm PCM (top PCM layer) is sputter deposited under the same conditions as the previous layer to form the top layer at the contact. Prior to deposition of this second PCM layer, the wafer surface is cleaned by an

in-situ Ar plasma pre-clean. The second PCM layer is then patterned to form the measurement structures. During patterning of the top layer, the bottom PCM layer is also masked. Hence these fabricated structures will have regions with a stack of a-PCM on top of c-PCM and regions with a-PCM only. The schematic representation of these structures is shown in Fig. 6.10. A top-view

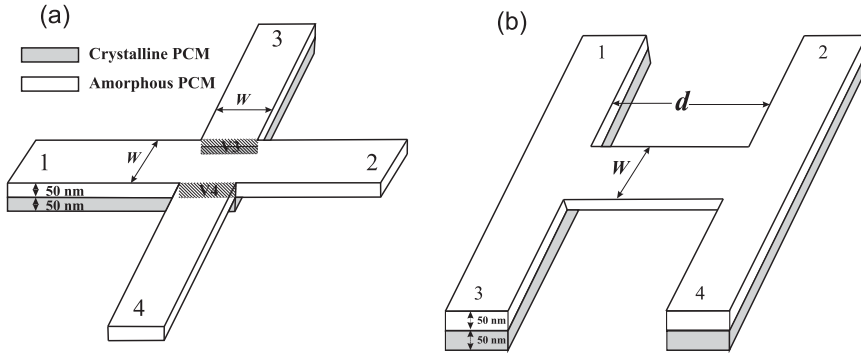


Figure 6.10: Schematic representation of a (a) CBKR structure and (b) TLM structure showing regions with a stack of c-PCM and a-PCM and regions with only a-PCM layers.

SEM image of the realized measurement structures is shown in Fig. 6.11. The regions with amorphous PCM and crystalline PCM (a-PCM+c-PCM) and regions with only amorphous PCM (a-PCM) are marked. To analyse the layers in the Kelvin structure, cross-sectional TEM images were taken along the dotted line marked in Fig. 6.11(a). This TEM analysis line is divided into three regions R1, R2 and R3 as depicted in the figure.

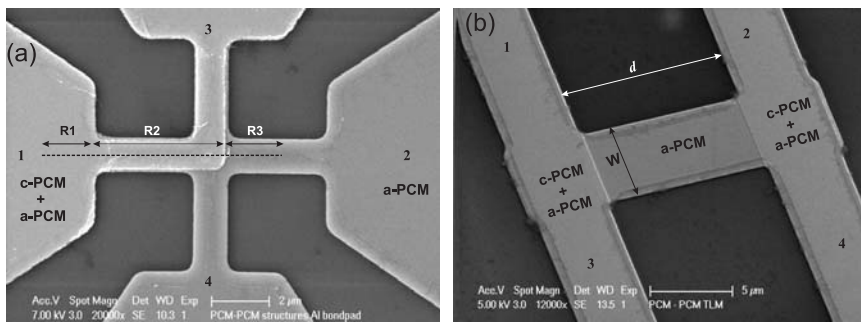


Figure 6.11: Top view SEM image of the (a) Kelvin resistor and (b) TLM structure showing the c-PCM+a-PCM regions and a-PCM regions. The dotted line in (a) represents the TEM analysis line for these structures.

### 6.2.1 Kelvin resistor measurements

The expected schematic cross-section of the Kelvin structures along the TEM line is shown in Fig. 6.12(a). To measure the electrical resistance of these structures, a current  $I$  is forced from 1 to 2 and the voltage  $V3$  and  $V4$  is measured at 3 and 4, respectively. From the measured resistance  $R_K=(V3-V4)/I$ ,  $\rho_{CP}$  can be calculated using eq. 2.9. The extracted  $\rho_{CP}$  with contact area is shown in Fig. 6.12(b). These structures were annealed for 5 minutes at different temperatures in the range from 120 °C to 300 °C. The extracted  $\rho_{CP}$  decreases by 5 orders of

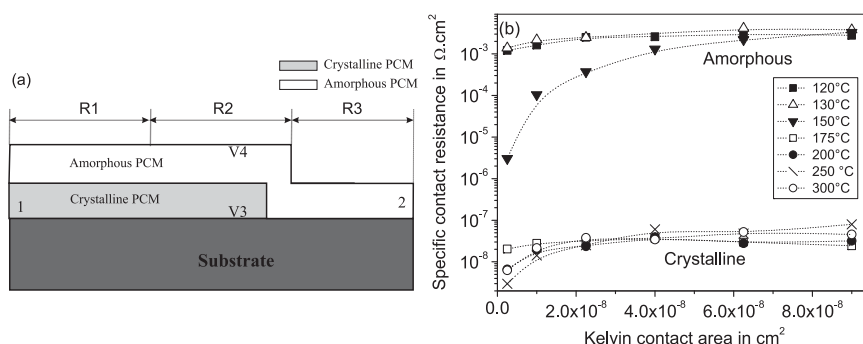


Figure 6.12: (a) Schematic cross-section of the Kelvin structures along the TEM line. (b) Extracted  $\rho_{CP}$  with contact area for the Kelvin structures.

magnitude after annealing the structures above 150 °C. This corresponds to the crystallization temperature of the PCM. In the amorphous state, the calculated  $\rho_{CP}$  is approximately  $2 \times 10^{-3} \Omega \cdot \text{cm}^2$ . This means that in a line cell, with a PCM layer thickness of 10 nm and a width of 100 nm in the reset state an  $R_{CP}$  of 200 M $\Omega$  per contact is obtained. This is unlikely high compared to the actual reset cell resistance of a few M $\Omega$ . Moreover, the measured  $\rho_{CP}$  values are above the measurement limit of approximately  $7.5 \times 10^{-5} \Omega \cdot \text{cm}^2$  [144][145]. In the crystalline state, the extracted  $\rho_{CP}$  is at the measurement limit ( $5 \times 10^{-9} \Omega \cdot \text{cm}^2$ ) of these structures for the smaller contacts.

### 6.2.2 TEM analysis

To further understand these measurements, cross-sectional TEM analysis was performed on Kelvin resistor structures along the (dotted) TEM line shown in Fig. 6.11(a). Along this analysis line, there are regions with a stack of c-PCM and a-PCM (R1 and R2) and with a-PCM layer only (R3). Prior to sample preparation and analysis, a carbon layer is deposited on the structures to prevent charging and a platinum layer to protect the sample during preparation in the focused ion beam. The reconstructed TEM image of the structures is shown in Fig. 6.13(a). In regions R1 and R2, a 50 nm a-PCM layer is sputter deposited on

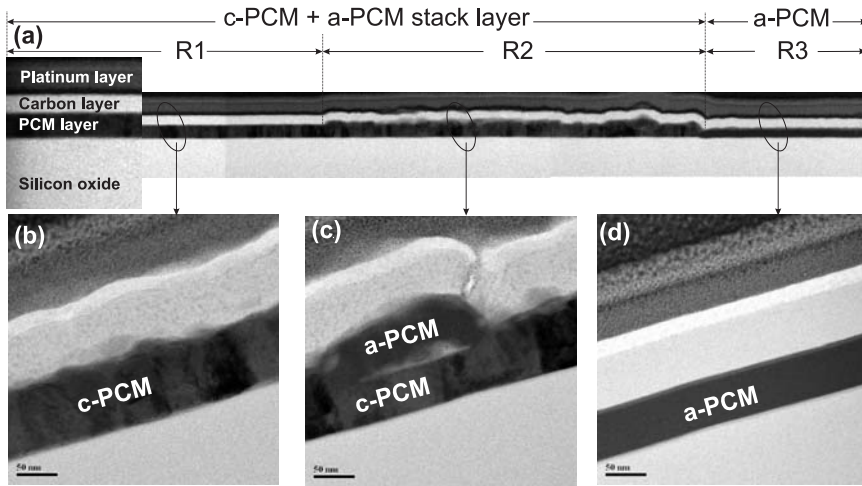


Figure 6.13: Reconstructed TEM image (not to scale) of the PCM layer. TEM image of; (a) a-PCM+c-PCM stack layer (b) without and (c) with re-deposited etch residues in between, (d) a-PCM layer deposited on SiO<sub>2</sub>.

top of the patterned c-PCM layer. The bottom c-PCM layer is patterned by RIE in an Ar/Cl plasma to reduce the effect of re-deposited sidewalls (explained in section 6.1). Nevertheless, re-deposited sidewalls formed during etching appeared after mask removal. This is observed as a thin brighter layer along the edges of the PCM layer in Fig. 6.11.

In region R1, the a-PCM is deposited on a clean c-PCM layer without re-deposition. From Fig 6.13(b) it shows the a-PCM layer becomes completely crystalline, despite the maximum thermal budget. The total PCM layer is slightly thinner because the Ar plasma pre-clean removes approximately 25 nm of the original c-PCM under-layer. In region R2, the re-deposition is clearly seen. During the Ar plasma pre-clean, the re-deposited layer is not completely removed and it masks the c-PCM under-layer from being cleaned. Subsequently, the PCM deposited on re-deposited residues remains amorphous, while in the other regions it partially turns into crystalline material. This results in an irregular and rough PCM top layer as shown in Fig. 6.13(c). Re-deposited residues are observed between the layers. In region R3, where the PCM layer is deposited directly on SiO<sub>2</sub>, a smooth a-PCM layer is observed from the TEM image in Fig. 6.13(d). No partial crystallization occurred.

In the case of Kelvin resistor structures, the contact region is formed in region R2. This region has a partially crystalline non uniform PCM layer and interfaces. Additional TEM images at different locations in this region are shown in Fig. 6.14. The presence of residues results in an undefined current distribution in the contact region. This leads to an increased measured voltage at the contact and

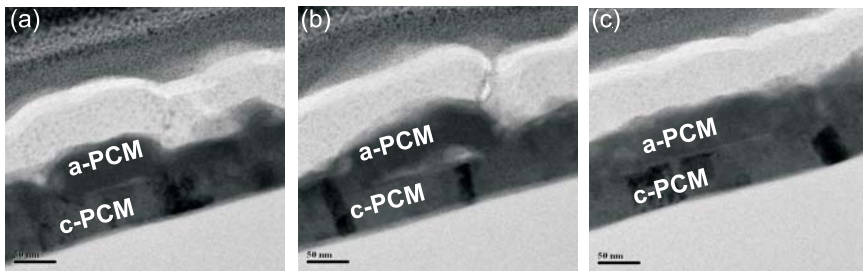


Figure 6.14: TEM images of different location in region R2.

high measured  $R_K$  values. Since the current spreading paths are also formed in the partially crystalline PCM regions, the exact dimension or geometry is not defined and the extraction of  $\rho_{CP}$  from these measured  $R_K$  values is not valid anymore.

To investigate the effect of further crystallization of the top PCM layer on  $R_K$  values, time-based measurements were performed on Kelvin resistor structures and Van der Pauw structures at a temperature lower than crystallization temperature of the PCM. The Van der Pauw structures were also fabricated with a stack of a-PCM on c-PCM layer along with the Kelvin resistor structure. The initial measured sheet resistance from these structures is  $82 \Omega/\square$ . The change in the sheet resistance of the structure with time when measured at  $120^\circ\text{C}$  is shown in Fig. 6.15(a). The sheet resistance decreases with time due to the further crystallization of the a-PCM layer. For Kelvin resistor, the change in  $R_K$  is shown in Fig. 6.15(b) for  $120^\circ\text{C}$  and  $125^\circ\text{C}$ . The contact area of the Kelvin structure is  $1 \mu\text{m}^2$ .

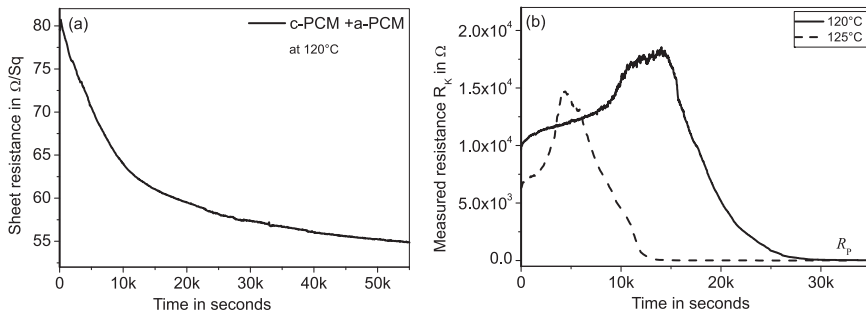


Figure 6.15: (a) Change in sheet resistance with time for of a-PCM+c-PCM layer measured at  $120^\circ\text{C}$  (b)  $R_K$  with time measured on Kelvin structures for three different temperatures.

In the Kelvin resistor, the measured resistance first increases and then decreases. This occurs earlier for the higher temperature. At the beginning of



the measurement, the current forced through these structures distributes itself non-uniformly in the contact region. This additional current spreading path overestimates the calculated  $R_K$  values. With time, this a-PCM starts to crystallize from the c-PCM to a-PCM interface, since doped-Sb<sub>2</sub>Te is a growth dominated material. Hence the c-PCM to a-PCM interface moves in the direction of the arrows as shown in Fig. 6.16(a). This increases the area of crystalline regions in the structure and it increases the current spreading path. This results in an increase in  $R_K$  as shown in Fig 6.15(b).

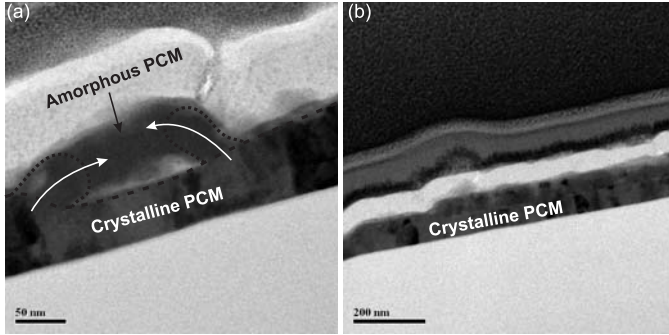


Figure 6.16: (a) movement of the crystallization front with time. (b) Fully crystalline PCM layer at the end of the measurement.

The subsequent decrease in  $R_K$  is associated with the complete crystallization of the PCM in the contact region. The measured resistance reaches a lower value and remains constant. At the end of the measurement, the PCM layer in these structure is completely crystalline as observed from the TEM image in Fig. 6.16(b).

### 6.2.3 TLM measurements

The fabricated TLM structure is shown in Fig. 6.11(b). It consists of c-PCM to a-PCM contacts separated with different spacing  $d$ . The contacts are fabricated such that the a-PCM layer is deposited on c-PCM layer with an Ar pre-clean in between, while the spacing is formed with an a-PCM layer on SiO<sub>2</sub>. After fabrication, the PCM layer in the spacing between the contacts remains amorphous, while at the contacts, it turns out that it is fully crystalline despite the lower thermal budget. Fig. 6.17(a) shows the cross-section TEM image of an interface showing the crystalline and amorphous regions. The schematic cross-section of the TLM structures is shown in Fig. 6.17(b). Contrary to an expected planar contact, these structures show two vertical c-PCM to a-PCM interfaces.

Electrical measurements were performed on these structures. The total measured resistance  $R_T$  is  $2R_{CP} + R_{PA}$ . The change in  $R_T$  with  $d$  for two different widths of the PCM line, measured at 20 °C is shown in Fig. 6.18(a). A linear



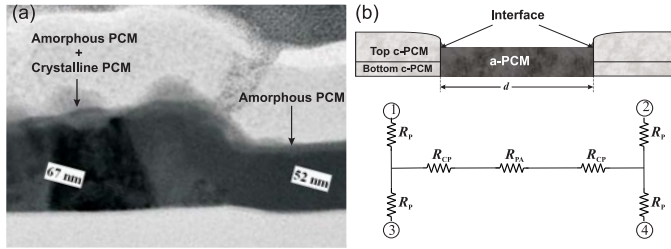


Figure 6.17: (a) TEM cross-section of the interface. (b) Schematic cross-section of the TLM structures showing the crystalline PCM and the amorphous PCM region. The interface between the two is also indicated along with the equivalent electrical network.

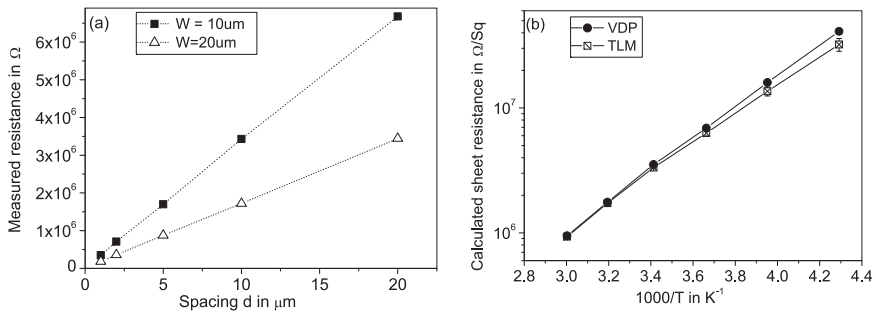


Figure 6.18: (a) Change in  $R_T$  with  $d$  for TLM structures. (b) Calculated a-PCM  $R_{SH}$  from TLM structure and from van der Pauw structures with temperature.

relationship is observed between  $R_T$  and  $d$  as described by eq. 2.14. From the slope of this curve, the sheet resistance of the PCM layer between the contacts can be calculated. Fig. 6.18(b) shows the calculated  $R_{SH}$  from the TLM measurements and those from amorphous PCM Van der Pauw structures measured in the temperature range from  $-40$  °C to  $60$  °C. The  $R_{SH}$  values for both measurement structures show good agreement. An exponential behavior is observed with temperature, from which an activation energy of  $0.26$  eV is calculated. This is the same value as determined for amorphous PCM in chapter 3. This shows that, the PCM between the contacts in the TLM structures is really in the amorphous state. Determination of  $l$  from  $R_T$  values in Fig. 6.18(a) however is impossible, since the c-PCM to a-PCM contacts formed are not lateral but vertical in nature.

## 6.3 Conclusion

In this chapter, we show that parasitic current paths formed in a measurement structure have a significant influence on the measured resistance values. Re-deposited sidewalls formed during argon etching result in the creation of par-

asitic current paths. The presence and influence of re-deposited PCM sidewalls on electrical resistance measurements and data extraction from Van der Pauw structures is modeled. CBKR structures with standing sidewalls leads to an underestimation of extracted  $\rho_c$ , due to inaccurate estimation of  $R_{SH}$  and  $\delta$ . The error introduced in extracted  $\rho_c$  with sidewalls is larger for CBKR structures with smaller contact area, smaller  $\delta$  and lower  $\rho_c$ . For these structures, the error introduced in electrical measurements is related to the pattern of the sidewalls. With re-deposited sidewalls, the resistance from Van der Pauw structures and contact resistance measurement from CBKR structures will be inaccurate. Re-deposited sidewalls results in an increased spread in measured resistance values, indicating its presence.

To characterize the crystalline PCM to amorphous PCM contacts, a modified Kelvin resistor and TLM structures were designed. Upon processing, the amorphous PCM crystallizes when deposited on clean crystalline PCM. Therefore the realization of a proper measurement structure was not possible. In addition, the formation of a partially crystalline non-uniform contact interface resulted in parasitic current paths. The experimental results are substantiated with TEM analysis of these structures.

## Conclusions and Recommendations

*This chapter summarizes the results obtained from this thesis work. The electrical contacts for phase change cells are characterized and modeled. Based on the experimental results optimization of the contacts in a phase change memory line cell is discussed. Recommendations for further research are included.*

## 7.1 Summary and conclusions

In this thesis, the electrical contacts for phase change memory cells are characterized and modeled. A phase change memory cell stores information by physical state changes of PCM, which is switched between the amorphous and crystalline state by resistive Joule heating. The most commonly used PCM for memory applications are the growth dominated doped-Sb<sub>2</sub>Te and nucleation dominated Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub>. For optimum power transfer during switching, the contact resistances  $R_C$  in the cell should be known together with the cell resistance  $R_L$ . Hence the knowledge of contact resistance values in terms of  $\rho_c$  is critical for scaling, design, modeling and optimization of switching characteristics of phase change memory cells.

In this work, Kelvin resistor structures (also CBKR) and transfer length method structures were fabricated to characterize the contacts in a phase change memory cell. The primary type of contact in a PCRAM cell is the electrode to PCM interface. TiW to doped-Sb<sub>2</sub>Te and Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> contact resistance measurements performed on these test structures resulted in similar  $\rho_c$  values both in the amorphous and crystalline states. The extracted  $\rho_c$  to amorphous doped-Sb<sub>2</sub>Te is approximately  $10^{-3} \Omega \cdot \text{cm}^2$  and to amorphous Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> is approximately  $10^{-2} \Omega \cdot \text{cm}^2$ . When measured with different CMOS compatible electrodes (W, TiW, Ta, TaN and TiN) to amorphous doped-Sb<sub>2</sub>Te, the extracted  $\rho_c$  for metal nitride electrodes ( $\rho_c \approx 10^{-4} \Omega \cdot \text{cm}^2$ ) is lower than for the corresponding metal electrodes ( $\rho_c \approx 10^{-3} \Omega \cdot \text{cm}^2$ ). In the crystalline state of the PCM, a  $\rho_c$  value of approximately  $2 \times 10^{-7} \Omega \cdot \text{cm}^2$  is extracted for TiW electrode to doped-Sb<sub>2</sub>Te and Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub>. There is no dependence with the work function of different electrode, and the values are in the same range ( $\rho_c \approx 10^{-7} \Omega \cdot \text{cm}^2$ ). Scaling of phase change memory line cells is possible by controlling the thickness of the PCM layer. When measured with different thickness of amorphous doped-Sb<sub>2</sub>Te layer, the average extracted  $\rho_c$  values increases from  $1.5 \times 10^{-4} \Omega \cdot \text{cm}^2$  for a 5 nm thick PCM layer to  $6 \times 10^{-3} \Omega \cdot \text{cm}^2$  for a thickness larger than 20 nm. In the crystalline state the extracted  $\rho_c$  values remain constant, this is approximately  $2.5 \times 10^{-7} \Omega \cdot \text{cm}^2$ . This  $\rho_c$  value is relevant for configuration of the contact geometry.

The electrical properties of the metal to PCM contacts in the amorphous and crystalline states show close similarities with metal to semiconductor contacts. In the amorphous state, the extracted  $\rho_c$  values exhibits a strong exponential dependence with measurement temperature. In addition a stronger dependence of  $\rho_c$  values with positive bias is observed as compared to negative bias. These  $\rho_c$  measurements and the calculated  $E_{00}$  values suggest that the charge transport at the metal to amorphous doped-Sb<sub>2</sub>Te interface is dominated by thermionic-field emission. The interface barrier formation at a metal to amorphous doped-Sb<sub>2</sub>Te interface is modeled with the presence of donor like and acceptor like defect states created in the PCM. Measurements performed on Kelvin structures with ultra-thin doped-Sb<sub>2</sub>Te layers indicated the existence of a modified region in the PCM at the interface, which is attributed to the dependence of  $\rho_c$  on the layer

thickness. In the crystalline state, the extracted  $\rho_c$  is almost independent on the measurement temperature as well as on polarity of applied bias voltage. Hall effect measurements performed indicate  $p$ -type conduction for both the PCM. The calculated carrier density is  $2 \times 10^{21} \text{ cm}^{-3}$  for crystalline doped-Sb<sub>2</sub>Te and  $5 \times 10^{20} \text{ cm}^{-3}$  for crystalline Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub>. When annealed at a higher temperature, the carrier concentration remains constant while the mobility increases. Based on this carrier concentration calculated  $E_{00}$  values and the  $\rho_c$  measurements indicate that charge transport mechanism at the metal to crystalline PCM interface is dominated by tunneling. With tunneling the  $\rho_c$  value is weakly dependent on the electrode work function.

To characterize the electrical contacts in the phase change memory cell at its operating frequency modified Scott TLM and linear TLM structures were designed and fabricated in the GSG configuration. Two port S-parameter measurements were performed on these test structures with frequencies up to 4 GHz. From the measured S-parameters, the contact impedance and  $\rho_c$  values are calculated with signal frequency.  $\rho_c$  values extracted from the GSG structures at low frequencies corresponds to the values obtained from identical test structures measured at DC in the four bond pad configuration. The metal to PCM interface is electrically modeled with a resistance in series with a parallel combination of capacitor and resistor. The frequency dependence of the contact impedance is attributed to the presence of the interfacial layer at the contact that acts like a capacitor. Comparing the frequency response of the measured contact impedances with the electrical model, the different resistor and capacitor values are extracted.

The formation of parasitic current paths can significantly influences the measured resistance values from test structures. In this work, the parasitic current paths formed due to re-deposited sidewalls formed during argon etching are investigated in detail. The presence and influence of re-deposited PCM sidewalls on electrical resistance measurements and data extraction from Van der Pauw structures is modeled. CBKR structures with standing sidewalls leads to underestimation of extracted  $\rho_c$  due to inaccurate estimation of  $R_{SH}$  and  $\delta$ . The error introduced in extracted  $\rho_c$  with sidewalls is larger for CBKR structures with smaller contact area, smaller  $\delta$  and lower  $\rho_c$ . Re-deposited sidewalls results in an increased spread in measured resistance values, indicating its presence.

Another type of contacts formed in a phase change memory cell is the crystalline PCM to amorphous PCM contacts. These contacts exist only in the reset state of the line cell. To characterize these contacts, a modified Kelvin resistor and TLM structures were designed. Upon processing, the amorphous PCM crystallizes when deposited on clean crystalline PCM. Therefore the realization of a proper measurement structure was not possible. In addition, the formation of a partially crystalline non-uniform contact interface resulted in parasitic current paths. The experimental results are substantiated with TEM analysis of these structures.

## 7.2 Recommendations

Electrodes to amorphous PCM contacts have a strong dependence on extracted  $\rho_c$  values with the polarity and magnitude of the applied bias voltage (Chapter 4). In addition, for ultrathin layer (5 nm) a modified region with different properties is observed in the PCM at the interface. These factors should be investigated in more detail for the switching of memory cells with electrode to amorphous PCM contacts.

In the reset state of a phase change memory cell, the crystalline PCM to amorphous PCM contacts discussed in chapter 6.2 can also be of relevance for cell properties. The attempt to characterize these contacts was hindered by fabrication limitations. A modified test structure or fabrication steps should be employed to fully characterize these interfaces.

# A

## Appendix

### A.1 Contact interface model

In the case of ohmic interfaces a physical model is derived to model the current transport. The interface is assumed as an infinitesimally thin layer, the total current density  $J$  is a function of the difference in the Fermi levels of the majority carrier on both sides of the interface:

$$J = J(v_m - v_s) = J(v_{ms}) \quad (\text{A.1})$$

where  $v_m$  is metal Fermi potential,  $v_s$  is semiconductor Fermi potential and  $v_{ms}$  is the potential difference. Then  $J$  expressed in a Maclaurin Series<sup>1</sup> as [52]:

$$J(v_{ms}) = J(0) + \frac{\partial J(v_{ms})}{\partial(v_{ms})} \Big|_{v_{ms}=0} v_{ms} + \frac{1}{2} \frac{\partial^2 J(v_{ms})}{\partial^2(v_{ms})} \Big|_{v_{ms}=0} v_{ms}^2 + \dots \quad (\text{A.2})$$

The first term is zero since there is no current at zero bias. For *ohmic* contacts, the second order and higher order terms are negligible. Then A.2 becomes linear:

$$J = \frac{v_{ms}}{\rho_c} \quad (\text{A.3})$$

where  $\rho_c$  is the specific contact resistance of the interface expressed as:

$$\rho_c = \left[ \frac{\partial J(v_{ms})}{\partial v_{ms}} \right]_{v_{ms}=0}^{-1} \quad (\text{A.4})$$

Physically  $\rho_c$  is the finite resistance seen by the infinitesimal current crossing the interface at an infinitesimal small potential difference. This is the physical parameter that governs steady state transport in *ohmic* contacts. At high current densities  $\rho_c$  is a weak function of  $v_{ms}$  due to other physical effects.

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<sup>1</sup>A Maclaurin series is a Taylor series expansion of a function about zero.

## A.2 Transmission Line Model

To calculate  $R_C$  and to extract  $\rho_c$ , the contact is modeled using transmission line equations assuming [51][146]:

- The current lines are normal to the metal to semiconductor interface.
- The thickness of the metal and diffusion layers can be neglected.
- The current-voltage characteristic of the contact is linear.

The equivalent circuit is as represented in Fig. A.1. The metal is assumed equipotential and the sheet resistance of metal is considered to be much lower than PCM sheet resistance.

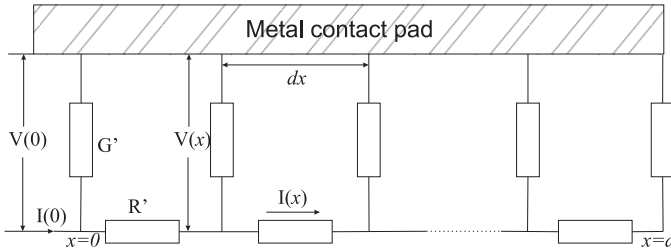


Figure A.1: Transmission line model equivalent circuit of a contact

The resistance  $R'$  and the conductance  $G'$  per unit length of the contact can be written as:

$$R' = \frac{R_{SH}}{W} \quad \& \quad G' = \frac{W}{\rho_c} \quad (\text{A.5})$$

The voltage and the current between the contacts at a distance  $x$  from the front edge of the contact is represented as:

$$\partial V_x = -R I_x \partial x \quad \& \quad \partial I_x = -G V_x \partial x \quad (\text{A.6})$$

Then the differential equation of the one - dimensional TLM follows :

$$\frac{\partial^2 V}{\partial x^2} - \frac{1}{l} = 0 \quad \& \quad \frac{\partial^2 I}{\partial x^2} - \frac{1}{l} = 0 \quad (\text{A.7})$$

By introducing the current  $I(0)$  and the voltage  $V(0)$  at the input of the transmission line, using this boundary conditions:

$$V(0) = V_0; I(0) = \left[ -\frac{1}{R'} \frac{\partial V(x)}{\partial x} \right]_{x=0} = I_0 \quad (\text{A.8})$$

The equations can be solved to get the voltage and the current in at the contact:

$$V(x) = V_0 \cosh\left(\frac{x}{l}\right) - Z I_0 \sinh\left(\frac{x}{l}\right) \quad (\text{A.9})$$



$$I(x) = I_0 \cosh\left(\frac{x}{l}\right) - \frac{V_0}{Z} \sinh\left(\frac{x}{l}\right) \quad (\text{A.10})$$

where, the characteristic impedance  $Z$  of the transmission line is represented as :

$$Z = R'l = \frac{R_{\text{SH}}l}{W} = \frac{\sqrt{\rho_c R_{\text{SH}}}}{W} \quad (\text{A.11})$$

In the equivalent circuit shown in Fig A.1,  $I(x) = 0$  for  $x > L$ . Hence, the current continuity requires that  $I(L) = 0$  and according to equation. We can define the contact resistance  $R_C$  as the input resistance of the transmission line given by:

$$R_C = \frac{V_0}{I_0} = Z \coth\left(\frac{L}{l}\right) \quad (\text{A.12})$$

The determination of the  $l$  can be further simplified in the case of electrically long contacts, with  $L \gg l$ :

$$R_C = Z = \frac{R_{\text{SH}}l}{W} \quad (\text{A.13})$$

The total resistance ( $R_T$ ) between a pair of identical contacts separated by a distance  $d$  then becomes:

$$R_T \approx \frac{R_{\text{SH}}d}{W} + \frac{2R_{\text{SH}}l}{W} = \frac{R_{\text{SH}}d}{W} + 2R_C \quad (\text{A.14})$$

### A.3 Hall effect measurements on *p*-type and *n*-type silicon

Calibration samples of *p*-type and *n*-type silicon for Hall measurements were prepared on Silicon on Insulator (SOI) wafers. The thickness of the silicon top layer is 600 nm. The wafers were implanted with boron for *p*-type doping and phosphorous for *n*-type doping. The implantation energy is selected to be 70 keV for both the dopants (Maximum for the system available in MiPlaza). The implantation dose  $\phi_i$ , number of implanted ions per unit area is represented as:

$$\phi_i = \frac{It}{qA} \text{ atoms/cm}^2 \quad (\text{A.15})$$

where,  $I$  is the beam current in  $A$ ,  $t$  is the implantation time in sec,  $A$  is the implant area in  $\text{cm}^2$  and  $q$  is the electronic charge. Using eq. A.15, for a layer thickness of 600 nm, to result in an  $N_C$  of  $5 \times 10^{19}/\text{cm}^3$  a  $\phi_i$  of  $3 \times 10^{15}/\text{cm}^2$ , and for  $N_C$  of  $3 \times 10^{20}/\text{cm}^3$  a  $\phi_i$  of  $18 \times 10^{15}/\text{cm}^2$  are calculated. Separate *p*-type and *n*-type calibration samples were prepared with high and low  $\phi_i$ . To allow for uniform dopant distribution throughout the silicon layer, after implantation the wafer is annealed at 1000 °C in  $\text{N}_2$  ambient for 10 hours. This procedure is deduced from SILVACO simulations. The expected value of  $N_C$  and the calculated  $N_C$  from  $\rho$  measurements is listed in Table A.1.

Table A.1: The calculated  $N_C$  (in  $\text{cm}^{-3}$ ) and  $\rho$  (in  $\Omega\cdot\text{cm}$ ) after different fabrication steps

Fabrication step		<i>p</i> -type silicon		<i>n</i> -type silicon	
		low	high	low	20 high
Implantation	$N_C$	$5 \times 10^{19}$	$3 \times 10^{20}$	$5 \times 10^{19}$	$3 \times 10^{20}$
After implantation and anneal	$\rho$	$1.92 \times 10^{-3}$	$7.2 \times 10^{-4}$	$1.26 \times 10^{-3}$	$3.72 \times 10^{-4}$
	$N_C$	$7 \times 10^{19}$	$2 \times 10^{20}$	$3 \times 10^{19}$	$2 \times 10^{20}$
Van der Pauw measurements	$\rho$	$2.15 \times 10^{-3}$	$8 \times 10^{-4}$	$1.4 \times 10^{-3}$	$4 \times 10^{-4}$
	$N_C$	$7 \times 10^{19}$	$2 \times 10^{20}$	$3 \times 10^{19}$	$2 \times 10^{20}$
Hall measurements	$N_C$	$7.68 \times 10^{19}$	$1.83 \times 10^{20}$	$5.28 \times 10^{19}$	$3.12 \times 10^{20}$

Subsequently Hall effect measurements were performed on these silicon samples. The current voltage measurements with and without magnetic field for both *p*-type and *n*-type samples are shown in Fig. A.2. The shift in  $I$ - $V$  character-

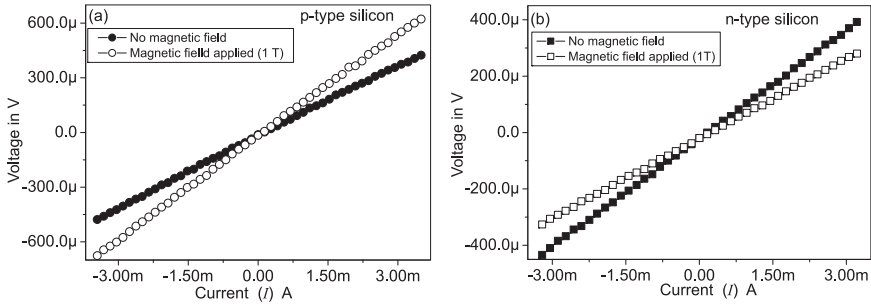


Figure A.2: Current-voltage measurements with and without magnetic field for *p*-type and *n*-type silicon samples.

istics and the polarity of  $V_H$  measured for PCM is identical to the characteristic observed for *p*-type silicon samples. The calculated  $N_C$  for silicon samples from Hall effect measurements and from  $\rho$  measurements show good agreement.

## A.4 Metal lift off process steps

Circular TLM structures have the advantage that these structures could be processed on blanket PCM layer without any isolation. To these structures were processed with a metal lift off process, using a lift off resist[147][148]. To fabricate these structures, first a 100 nm PCM is deposited amorphously by DC magnetron sputtering on a clean oxidized silicon wafer. Then the wafer surface is coated with a 600 nm LOR (lift off resist) resist with a spin speed of 2000 rpm, which is

subsequently baked on a hotplate at 120 °C for 2 minutes. After that the wafer surface is coated with a 1.3  $\mu\text{m}$  HPR 504 resist spin at 4000 rpm and is baked at 90 °C for 2 minutes. The resist bake temperature determines the thermal budget, which should be lower than the crystallization temperature of the PCM used. The wafer is then exposed to UV light with the circular TLM mask (8sec at 950 Watts). HPR 504 resist which is sensitive to light will be modified exposure to light. These exposed parts are then developed in a metal ion based (MIB) PLSI developer for 70 sec. LOR is insensitive to UV exposure but will be etched in PLSI. When etched long enough an undercut pattern is obtained with the resist stack which is essential for metal liftoff. The etch rate of LOR resist in PLSI also depends on the baking temperature. The SEM image of the undercut patterns formed when the LOR is baked at different temperatures  $T$ , of 120 °C, 150 °C and 175 °C is shown in Fig. A.3. Subsequently the developing time  $t$ , in PLSI is also different.

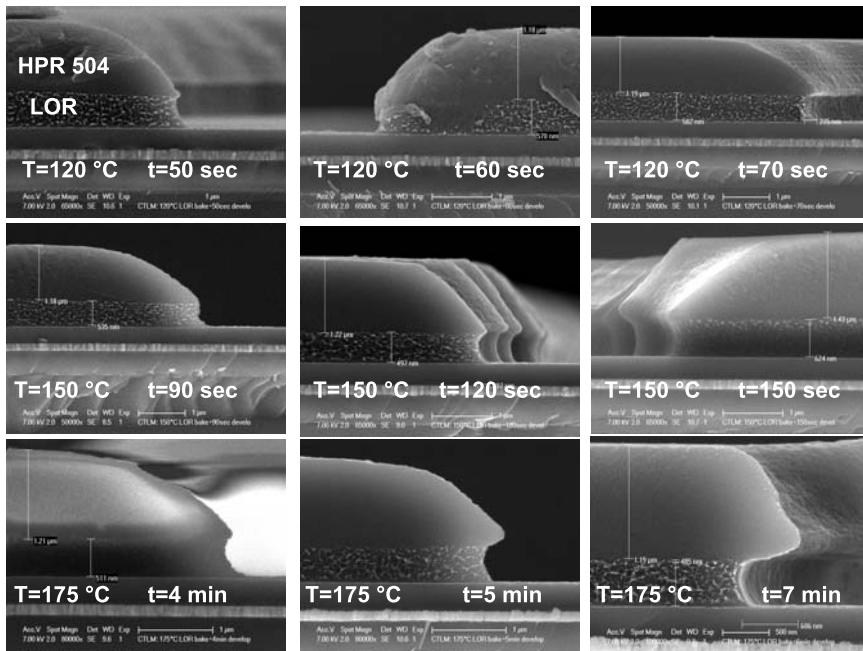


Figure A.3: Lift off process showing the formation of resist undercut for different baking temperature with the subsequent developing times.

A 50 nm TiW and 250 nm Al is then deposited with a soft sputter etch (remove 2nm oxide) prior to metal deposition. The resist is then removed with metal lift off in a megasonic acetone bath. Without a proper undercut developed in the resist layer the metal will not be lifted off. The situation with and without metal lift off is shown in Fig. A.4.

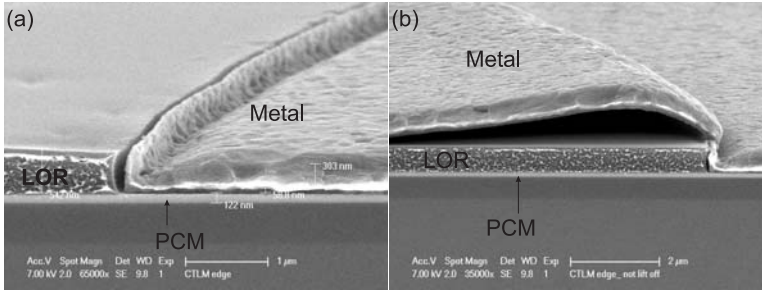


Figure A.4: Situation with and without metal lifted off.

## A.5 I-V-T measurements

In the case when  $V \gg k_b T/q$ , then eq.2.5 for the total current through the junction with thermionic emission is expressed as [31][44]:

$$\ln \left[ \frac{I}{T^2} \right] = \ln(AA^*) - \left[ \frac{q(\phi_b - V)}{k_b T} \right] \quad (\text{A.16})$$

For a given bias from the plot of  $\ln(I/T^2)$  versus  $1/T$  for TiW to doped-Sb<sub>2</sub>Te contacts with a contact area of  $1 \mu\text{m}^2$  in the amorphous state is shown in Fig. A.5. The slope of this curve  $-q(\phi_b - V)$  is the activation energy from which the

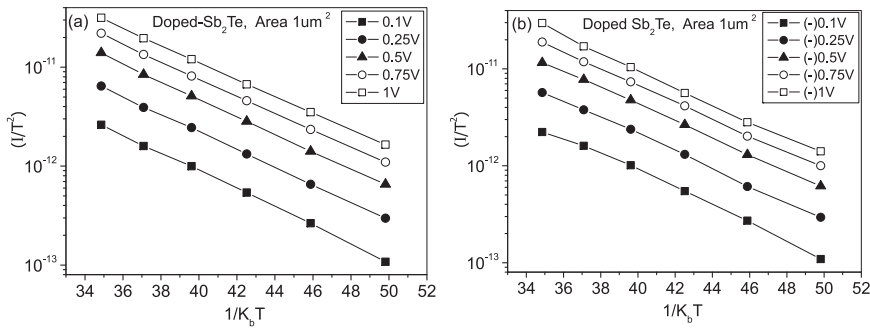


Figure A.5: Plot of  $\ln(I/T^2)$  with temperature for (a) positive voltage and (b) negative voltage.

barrier height is determined. The value of effective Richardson's constant can be obtained from the intercept at  $1/T=0$ . This determined activation energy for positive and negative voltage across the contact for both the PCM is shown in Fig. A.6.

As observed from the Fig. A.6 the calculated activation energy decreases with increase in positive voltage at the contact, while remains constant for negative

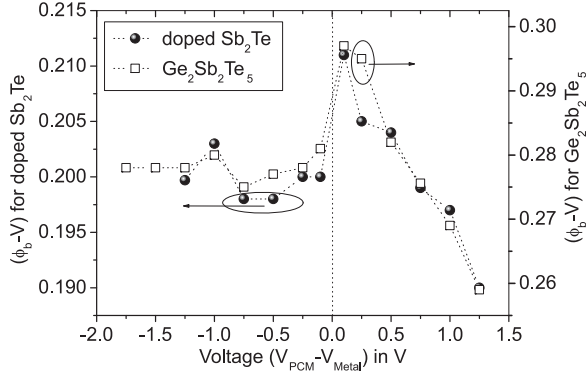


Figure A.6: Calculated activation energy ( $E_A$ ) for positive and negative voltage bias across the contact with PCM in the amorphous state.

voltages. A positive voltage ( $V_{\text{PCM}} - V_{\text{Metal}}$  positive) implies a higher potential on the PCM side relative to the metal. Since PCM behaves like a  $p$ -type material, with a positive potential the metal-PCM junction is forward biased. Hence with a larger positive bias the holes can move easily from PCM to metal. With a negative potential at the contact, the barrier for carriers moving from the metal to the PCM remains the same and hence the current is unaffected by the applied voltage. Note that this extracted activation energy is slightly lower than the activation energy calculated from specific contact resistance. The barrier height cannot be estimated from these measurements since the extracted activation energy do not scale with the applied forward bias. Furthermore the intercept at the lowest bias results in approximately -19 to -17.5 for both the PCM. This value slightly decreases with increase in bias. The contact area,  $A$  is  $(900 \text{ nm} \times 900 \text{ nm}) 0.81 \times 10^{-8} \text{ cm}^2$ . From this calculated value of Richardson's constant  $A^*$  varies between  $0.69 \text{ A/cm}^2 \cdot \text{K}^2$  to  $3.4 \text{ A/cm}^2 \cdot \text{K}^2$ .

## A.6 Test structure fabrication; process-flow

- Clean silicon wafer with 500 nm silicon oxide (starting substrate)
- Alignment marker formation
  - Resist spin (HPR 504) + Lithography (marker windows) + Resist developing + Bake at  $90^\circ \text{C}$  for 10min
  - Wet etching of 500 nm SiO<sub>2</sub> in Buffered Oxide Etch (BOE)
  - Resist removal with acetone
  - Resist spin (HPR 504) + Lithography (allignment markers) + Resist developing
  - Dry etch of markers in Si -  $150 \mu\text{m}$

- Resist removal in Oxygen plasma
- Bottom metal electrode formation
  - 100 nm TiW deposition by sputtering
  - Resist spin (SPR) + Lithography (Mask Angel -BE) with an Energy of  $240 \text{ mJ/cm}^2$  + Resist developing
  - Metal etching (to form the electrical connection layout and the test structures)
  - Resist mask removal
- 300 nm PECVD oxide deposition (3 times the step height of metal)
- Chemical Mechanical Polishing (CMP)
- Clearing of bondpads (in case to clear oxide from the bondpads)
  - Resist spin + Lithography (Mask Angel -CB) + Resist developing
  - Wet etching of  $\text{SiO}_2$  in Buffered Oxide Etch (BOE) + resist mask removal
- Bond pad formation (if the PCM should be amorphous in the device)
  - Ar preclean
  - 500nm Al or 100nm TiW deposition by sputtering
  - Resist spin + Lithography (Mask Angel -IN) + Resist developing + Bake at  $90 \text{ }^\circ\text{C}$  for 10min
  - Al etching in PES etch + resist mask removal
- Sputter etching (Ar preclean)
  - Wafer 1 - Ar pre-clean equivalent to removal of 5 nm of  $\text{SiO}_2$
  - Wafer 2 - No Ar Pre-clean
  - Wafer 3 - No Ar Pre-clean + Desum in Oxygen plasma at  $110 \text{ }^\circ\text{C}$  for 5 minutes
- PCM deposition 50 nm sputtering
- PCM patterning to form top layer
  - Resist spin + Lithography (Mask Angel -PCM) + Resist developing
  - Dry etching of PCM in Cl:Ar plasma + Resist mask removal

## Bibliography

- [1] S. Asai, "Semiconductor memory trends," *Proceedings of the IEEE*, vol. 74, no. 12, pp. 1623–1635, Dec. 1986.
- [2] "Assessment of the potential and maturity of selected emerging research memory technologies," International Technology Roadmap for Semiconductors, Tech. Rep., 2010. [Online]. Available: <http://www.itrs.net/Links/2010ITRS/Home2010.htm>
- [3] A. Chung, J. Deen, J.-S. Lee, and M. Meyyappan, "Nanoscale memory devices," *Nanotechnology, Tropical review*, vol. 21, no. 41, p. 412001, 2010.
- [4] Y. Fujisaki, "Current status of nonvolatile semiconductor memory technology," *Jap. J. Appl. Phys, comprehensive rev.*, vol. 49, p. 100001, 2010.
- [5] M. H. R. Lankhorst, B. W. S. M. M. Ketelaars, and R. A. M. Wolters, "Low-cost and nanoscale non-volatile memory concept for future silicon chips," *Nature Materials*, vol. 4, pp. 347–352, Apr. 2005.
- [6] C. H. Lam, "The quest for the universal semiconductor memory," in *IEDM Tech. Dig.*, Dec. 2005, pp. 327–331.
- [7] K. Attenborough, G. A. M. Hurkx, R. Delhougne, J. Perez, M. T. Wang, T. C. Ong, L. Tran, D. Roy, D. Gravesteijn, and M. van Duuren, "Phase change memory line concept for embedded memory applications," in *IEDM Tech. Dig.*, Dec. 2010, pp. 648–651.
- [8] S. Raoux and M. Wuttig, *Phase change materials: Science and application*. Springer Verlag, 2009.
- [9] E. R. Meinders, A. V. Mijiritskii, L. van Pieterse, and M. Wuttig, *Optical Data Storage: Phase-change Media and Recording*. The Netherlands: Springer, 2006, no. 1-402-04216-7.
- [10] S. R. Ovshinsky, "Reversible electrical switching phenomena in disordered structures," *Phys. Rev. Lett.*, vol. 21, no. 20, pp. 1450–1453, 1968.
- [11] R. G. Neale, D. L. Nelson, and G. E. Moore, "Nonvolatile and reprogrammable, the read mostly memory is here," *Electronics*, pp. 56–60, Sept. 1970.
- [12] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, pp. 114–117, Apr. 1965.
- [13] H. S. P. W. et .al., "Phase change memory," *Proceedings of the IEEE*, vol. 98, no. 12, pp. 2201–2227, Dec. 2010.

- [14] G. W. Burr, M. J. Breitwisch, M. Franceschini, D. Garetto, K. Gopalakrishnan, B. Jackson, B. Kurdi, C. Lam, L. A. Lastras, A. Padilla, B. Rajendran, S. Raoux, , and R. S. Shenoy, "Phase change memory technology," *J. Vac. Sci. Technol. B*, vol. 28, no. 2, pp. 223–262, Mar. 2010.
- [15] S. Lai, "Current status of the phase change memory and its future," in *IEDM Tech. Dig.*, Dec. 2003, pp. 255–258.
- [16] S. Demuynck, A. Nackaerts, G. V. den bosch, T. Chiarella, J. Ramos, Z. Tokei, J. Vaes, N. Heylen, G. P. Beyer, M. V. Hove, T. Mandrekar, and R. Schreutelkamp, "Impact of Cu contacts on front-end performance: a projection towards 22 nm node," in *International Interconnect Technology Conference*, June 2006, pp. 178–180.
- [17] D. L. Kencke, I. V. Karpov, B. G. Johnson, S. J. Lee, D. Kau, S. J. Hudgens, J. P. Reifenberg, S. D. Savransky, J. Zhang, M. D. Giles, and G. Spadini, "The role of interfaces in damascene phase-change memory," in *IEDM Tech. Dig.*, Dec. 2007, pp. 323–326.
- [18] D. H. Kang, I. H. Kim, J. hyun Jeong, B. ki Cheong, D. H. Ahn, D. Lee, H. M. Kim, K. B. Kim, and S. H. Kim, "An experimental investigation on the switching reliability of a phase change memory device with and oxidized TiN electrode," *J. Appl. Phys.*, vol. 100, p. 054506, 2006.
- [19] H. H. Berger, "Models for contacts to planar devices," *Solid-state Elec.*, vol. 15, pp. 145–158, 1972.
- [20] H. H. Berger, "Contact resistance and contact resistivity," *J. Electrochem. Soc.: Solid-State science and Tech.*, vol. 119, no. 4, pp. 507–514, 1972.
- [21] I. F. Chang, "Contact resistance in diffused resistors," *J. Electrochem. Soc.: Solid-State science and Tech.*, vol. 179, no. 3, pp. 368–372, 1970.
- [22] R. Holm, *Electric contacts*. Springer-verlag, Berlin, 1967.
- [23] C. Ting and C. Chen, "A study of the contacts of a diffused resistor," *Solid St. Electron.*, vol. 14, pp. 433–438, 1971.
- [24] C. Y. Change, Y. K. Fang, and S. M. Sze, "Specific contact resistance of metal-semiconductor barriers," *Solid-State Elect.*, vol. 14, pp. 541–550, 1971.
- [25] R. H. Fowler and E. A. Guggenheim, *Statistical thermodynamics*. England: Cambridge university press, 1939.
- [26] E. H. Rhoderick and R. H. Williams, *Metal-semiconductor contacts*, 2nd ed. Oxford: Clarendon press, 1988.
- [27] W. Schottky, "Halbleitertheorie der sperrschicht," *Naturwissenschaften*, vol. 26, p. 843, 1938.
- [28] W. H. Schottky, "Zur halbleitertheorie der sperrschicht und spi," *Naturwissenschaften Z. Phys.*, vol. 113, pp. 367–414, July 1939.
- [29] W. Schottky, "Vereinfachte und erweiterte theorie der randschichtgleichrichter," *Naturwissenschaften Z. Phys.*, vol. 118, pp. 539–592, Feb. 1942.
- [30] N. F. Mott, "Note on the contact between a metal and an insulator or semiconductor," *Proc. Camb. Philos. Soc.*, vol. 34, p. 568, 1938.
- [31] S. M. Sze, *Physics of semiconductor devices*, 2nd ed. New York: Wiley-Interscience, 1981.
- [32] F. A. Padovani and R. Saratton, "Field and thermionic field emission in schottky barriers," *Solid-State Elect.*, vol. 9, pp. 695–707, 1966.
- [33] A. Y. C. Yu, "Electron tunneling and contact resistance of metal-silicon contact barriers," *Solid St. Electron.*, vol. 13, pp. 239–247, 1970.
- [34] D. K. Schroder and D. L. Meier, "Solar cell contact resistance-a review," *IEEE Trans. Electron Devices*, vol. 31, pp. 637–647, May 1984.



- [35] F. A. Kroger, G. Diemer, and H. A. Klasens, "Nature of an ohmic metal-semiconductor contact," *Phys. Rev.*, vol. 103, no. 2, p. 279, 1956.
- [36] W. Schottky, "Encyclopædia britannica online." Encyclopædia Britannica., Tech. Rep. [Online]. Available: [www.britannica.com/EBchecked/topic/528213/Walter-Schottky](http://www.britannica.com/EBchecked/topic/528213/Walter-Schottky)
- [37] S. J. Proctor and L. W. Linholm, "A direct measurement of interfacial contact resistance," *IEEE Electron Device Lett.*, vol. 3, pp. 294–296, Oct. 1982.
- [38] W. Shockley, "Research and investigation of inverse epitaxial UHF power transistors," Air Force Atomic Laboratory, Wright-Patterson Air Force base, Ohio, Tech. Rep. Rep.AL-TOR-64-207, sept. 1964.
- [39] D. P. Kennedy and P. C. Murley, "A two dimensional mathematical analysis of the diffused semiconductor resistor," *IBM J. Res. and Dev.*, vol. 12, pp. 242–250, 1968.
- [40] H. H. Berger, "Contact resistance on diffused resistors," in *ISSCC Dig. Tech.*, 1969, p. 160.
- [41] H. Murrmann and D. Widmann, "Current crowding on metal contacts to planar devices," in *ISSCC Tech. Dig.*, 1969, p. 162.
- [42] H. Murrmann and D. Widmann, "Current crowding on metal contacts to planar devices," *IEEE Trans. Electron Devices*, vol. 16, pp. 1022–1024, Mar. 1969.
- [43] H. Murrmann and D. Widmann, "Messung des ubergangswiderstandes zwischen metal und diffusionsschicht in si-planarelementen," *Solid-State Elect.*, vol. 12, p. 879, 1969.
- [44] D. K. Schroder, *Semiconductor material and device characterization*, 3rd ed. Wiley-Interscience, 2006.
- [45] M. Finetti, A. Scorzoni, and G. Soncini, "Lateral current crowding effects on contact resistance measurement in four terminal resistor test patterns," *IEEE Electron Devices Lett.*, vol. 5, no. 12, pp. 524–526, Dec. 1984.
- [46] W. M. Loh, K. Saraswat, and R. W. Dutton, "Analysis and scaling of kelvin resistors for extraction of specific contact resistivity," *IEEE Electron Device Lett.*, vol. 6, pp. 105–107, Mar. 1985.
- [47] J. G. J. Chern and W. G. Oldham, "Determining specific contact resistivity from contact end resistance measurements," *IEEE Electron Device Lett.*, vol. 5, no. 5, pp. 178–180, May 1984.
- [48] W. M. Loh, S. E. Swirhun, E. Crabbe, K. Saraswat, and R. M. Swanson, "An accurate method to extract specific contact resistivity using cross-bridge kelvin resistors," *IEEE Electron Device Lett.*, vol. 6, pp. 441–443, Sept. 1985.
- [49] T. A. Schreyer and K. C. Saraswat, "A two dimensional analytical model of the cross bridge kelvin resistor," *IEEE Electron Device Lett.*, vol. 7, pp. 661–663, Dec. 1986.
- [50] D. L. Meier and D. K. Schroder, "Contact resistance: its measurement and relative importance to power loss in a solar cell," *IEEE Trans. Electron Devices*, vol. 31, no. 5, pp. 647–653, May 1984.
- [51] D. B. Scott, W. R. Hunter, and H. Shichijo, "A transmission line model for silicided diffusions: Impact on the performance of the VLSI circuits," *IEEE Trans. Electron Devices*, vol. 29, no. 4, pp. 651–661, Apr. 1982.
- [52] W. M. Loh, S. E. Swirhun, T. A. Schreyer, R. M. Swanson, and K. C. Saraswat, "Modeling and measurement of contact resistances," *IEEE Electron Device Lett.*, vol. 6, pp. 441–443, Sept. 1985.
- [53] G. K. Reeves and H. B. Harrison, "Obtaining the specific contact resistance transmission line model measurements," *IEEE Electron Device Lett.*, vol. 3, no. 5, pp. 111–113, May 1982.

- [54] G. K. Reeves, "Specific contact resistance using a circular transmission line model," *Solid-State Elect.*, vol. 23, pp. 487–490, 1980.
- [55] D. B. Scott, R. A. Chapman, C.-C. Wei, S. S. Mahant-Shetti, R. A. Haken, and T. C. Holloway, "Titanium disilicide contact resistivity and its impact on 1- $\mu\text{m}$  CMOS circuit performance," *IEEE Trans. Electron Devices*, vol. 34, pp. 562–574, Mar. 1987.
- [56] J. H. Klootwijk and C. E. Timmering, "Merits and limitation of circular TLM structures for contact resistance determination for novel III-V HBTs," in *IEEE International Conference on Microelectronic Test Structures (ICMTS)*, vol. 17, Mar. 2004, pp. 247–252.
- [57] L. F. Lester, J. M. Brown, J. C. Ramer, L. Zhang, S. D. Hersee, and J. C. Zolper, "Non-alloyed Ti/Al ohmic contacts to n-type GaN using high temperature pre-metallization anneal," *Appl. Phys. Lett.*, vol. 69, no. 18, pp. 2737–2739, Oct. 1996.
- [58] G. S. Marlow and M. B. Das, "The effect of contact size and non-zero metal resistance on the determination of specific contact resistance," *Solid-State Electron.*, vol. 25, pp. 91–94, 1982.
- [59] D. Roy, R. M. T. Pijper, L. F. Tiemeijer, and R. A. Wolters, "Contact resistance measurement structures for high frequencies," in *24<sup>th</sup> International Conference on Microelectronic Test Structures (ICMTS)*, Apr. 2011, pp. 49–54.
- [60] D. M. Pozar, *Microwave engineering*, 3rd ed. John Wiley & Sons. Inc., 2005.
- [61] S. S. Cohen, "Contact resistance and methods for its determination," *Thin Solid Films*, vol. 104, no. 3-4, pp. 361–379, June 1983.
- [62] S. J. Proctor, L. Linholm, and J. A. Mazer, "Direct measurement of interfacial contact resistance end contact resistance and interfacial contact layer uniformity," *IEEE Trans. Electron Devices*, vol. 30, no. 11, pp. 1535–1542, Nov. 1983.
- [63] N. Stavitski, J. H. Klootwijk, H. W. V. Zeijl, A. Y. Kovalgin, and R. A. M. Wolters, "Cross bridge kelvin resistor structure for reliable measurement of low contact resistances and contact interface characterization," *IEEE Trans. Semiconduct. Manufact.*, vol. 22, pp. 146–152, Feb. 2009.
- [64] S. Oussalah, B. Djeddar, and R. Jerisian, "A comparative study of different contact resistance test structures dedicated to the power process technology," *Solid-State Elect.*, vol. 49, no. 10, pp. 1617–1622, 2005.
- [65] D. Roy, M. A. A. Zandt, C. E. Timmering, J. H. Klootwijk, and R. A. M. Wolters, "Contact resistance of phase change materials to TiW electrodes in amorphous and crystalline state," in *IEEE Non Volatile Memory Tech. Symp. (NVMTS)*, Oct. 2009, pp. 12–15.
- [66] L. J. van der Pauw, "A method of measuring specific resistivity and hall effect of discs of arbitrary shape," *Philips Research Reports*, vol. 13, no. 1, pp. 1–9, Feb. 1958.
- [67] G. Zhou, H. J. Borg, J. C. N. Rijpers, M. H. R. Lankhorst, and J. J. L. Horikx, "Crystallization behavior of phase-change materials: comparison between nucleation- and growth-dominated crystallization," in *Proc. Of SPIE*, vol. 4090, 2000, pp. 108–115.
- [68] I. Friedrich, V. Weidenhof, N. Njoroge, P. Franz, and M. Wuttig, "Structural transformations of  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  films studied by electrical resistance measurements," *J. Appl. Phys.*, vol. 87, no. 9, pp. 4130–4134, May 2000.
- [69] N. F. Mott and E. A. Davis, *Electronic processes in non-crystalline materials*, 2nd ed. Oxford: Clarendon Press, 1979.
- [70] L. van Pieterse, M. van Schijndel, J. C. N. Rijpers, and M. Kaiser, "Te-free, Sb-based phase-change materials for high-speed rewritable optical recording," *Appl. phys. lett.*, vol. 83, no. 7, pp. 1373–1375, Aug. 2003.
- [71] M. L. Lee, L. P. Shi, Y. T. Tian, C. L. Gan, , and X. S. Miao, "Crystallization behaviour of  $\text{Sb}_7\text{OTe}_3$  and  $\text{Ag}_3\text{In}_5\text{Sb}_6\text{OTe}_3$  chalcogenide materials for optical media applications," *phys. stat. sol. A*, vol. 205, no. 2, pp. 340–344, 2008.

- [72] J. Tauc, R. Girgorovici, and A. Vancu, "Optical and electronic properties of amorphous germanium," *Physica. Status. Solidi.*, vol. 15, pp. 627–637, 1966.
- [73] B.-S. Lee, J. R. Abelson, S. G. Bishop, D.-H. Kang, B. ki Cheong, and K.-B. Kim, "Investigation of the optical and electronic properties of  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  phase change material in its amorphous, cubic, and hexagonal phases," *J. of Applied Physics*, vol. 97, p. 093509, 2005.
- [74] E. H. Hall, "On a new action of the magnet on the electric current," *American Journal of Mathematics*, vol. 2, pp. 287–292, 1879.
- [75] H.-K. Lyeo, D. G. Cahill, B.-S. Lee, J. R. Abelson, M.-H. Kwon, K.-B. Kim, S. G. Bishop, and B. ki Cheong, "Thermal conductivity of phase-change material  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ ," *Appl. Phys. Lett.*, vol. 89, p. 151904, 2006.
- [76] R. L. Gillenwater, M. J. Hafich, and G. Y. Robinson, "Extraction of the minimum specific contact resistivity using kelvin resistors," *IEEE Electron Device Lett.*, vol. 7, no. 12, pp. 674–676, Dec. 1986.
- [77] J. C. Male, "Hall effect measurement in semiconducting chalcogenide glasses and liquids," *Brit. J. Appl. Phys.*, vol. 18, pp. 1543–1549, 1967.
- [78] S. A. Baily, D. Emin, and H. Li, "Hall mobility of amorphous  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ ," *Solid state communication*, vol. 139, pp. 161–164, 2006.
- [79] R. Yokota, "Electronic dielectric constants of crystalline and amorphous  $\text{GeSb}_2\text{Te}_4$  and  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  semiconductors," *Jap. J. Appl. Phys.*, vol. 28, no. 8, pp. 1407–1411, Aug. 1989.
- [80] S. W. Ryu, J. H. Lee, Y. B. Ahn, C. H. Kim, B. S. Yang, G. H. Kim, S. G. Kim, S.-H. Lee, C. S. Hwang, and H. J. Kim, "The reason for the increased threshold switching voltage of  $\text{SiO}_2$  doped  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  thin films for phase change random access memory," *Appl. Phys. Lett.*, vol. 95, 112110, 2009.
- [81] D. Ielmini and Y. Zhang, "Analytical model for subthreshold conduction and threshold switching in chalcogenide-based memory devices," *J. Appl. Phys.*, vol. 102, p. 054517, 2007.
- [82] C. B. Thomas, "The temperature dependence of the non-ohmic current and switching characteristics of a chalcogenide glass," *J. Phys. D: Appl. Phys.*, vol. 9, pp. 2587–2596, 1976.
- [83] C. R. Crowell and V. L. Reideout, "Thermionic field resistance maxima in metal semiconductor (schottky) barriers," *Appl. Phys. Lett.*, vol. 14, no. 3, pp. 85–88, 1969.
- [84] R. C. West, *CRC handbook of chemistry and physics*, 64th ed. CRC Press inc. Florida, 1983-1984.
- [85] C. S. Bhatia and M. K. Sinha, "Adsorption and surface diffusion of titanium on tungsten in a field emission microscope," *Surface Science*, vol. 43, pp. 369–384, 1974.
- [86] B. Y. Tsui and C.-F. Huang, "Wide range work function modulation of binary alloys for MOSFET application," *IEEE Electron Device Lett.*, vol. 24, no. 3, pp. 153–155, Mar. 2003.
- [87] B. Claffin, M. Binger, and G. Lucovsky, "Interface studies of tungsten nitride and titanium nitride composite metal gate electrodes with thin dielectric layers," *J. Vac. Sci. Technol. A*, vol. 16, no. 3, pp. 1757 – 1761, May 1998.
- [88] B. P. Luther, S. E. Mohney, and T. N. Jackson, "Titanium and titanium nitride contacts to n-type gallium nitride," *Semicond. Sci. Technol.*, vol. 13, pp. 1322–1327, 1998.
- [89] J. Westlinder, G. Sjoblom, and J. Olsson, "Variable work function in MOS capacitors utilizing nitrogen-controlled  $\text{TiN}_x$  gate electrodes," *Microelectronic Engineering*, vol. 75, pp. 389–396, 2004.

- [90] C. S. Kang, H. J. Cho, Y. H. Kim, R. Choi, K. Onishi, A. Shahriar, and J. Lee, "Characterization of resistivity and work function of sputtered-TaN film for gate electrode applications," *J. Vac. Sci. Technol. B*, vol. 21, no. 5, pp. 2026–2028, Sept. 2003.
- [91] E. Vieujot-Testemale, J. Palau, A. Ismail, and L. Lassabatere, "Properties of the contact on ion cleaned n and p type silicon surfaces," *Solid-state Electronics*, vol. 26, no. 4, pp. 325–331, 1983.
- [92] S. J. Fonash, S. Ashok, and R. Singh, "Effect of neutral ion beam sputtering and etching on silicon," *Thin Solid Films*, vol. 90, pp. 231–235, 1982.
- [93] W. E. Spicer, I. Lindau, P. Skeath, C. Y. Su, and P. Chye, "Unified mechanism for schottky-barrier formation and III-V oxide interface states," *Phys. Rev. Lett.*, vol. 44, no. 6, pp. 420–423, 1980.
- [94] J. Tersoff, "Schottky barrier height and the continuum of gap states," *Phys. Rev. Lett.*, vol. 52, no. 6, pp. 465–468, 1984.
- [95] R. A. Street and N. F. Mott, "States in the gap in glassy semiconductors," *Phys. Rev. Lett.*, vol. 35, no. 19, pp. 1293–1296, 1975.
- [96] A. Pirovano, A. L. Lacaita, A. Benvenuti, F. Pellizzer, and R. Bez, "Electronic switching in phase-change memories," *IEEE Trans. Elect. Devices*, vol. 51, no. 3, pp. 452–459, Mar. 2004.
- [97] A. V. Kolobov, "On the origin of p-type conductivity in amorphous chalcogenides," *J. of Non-Crystalline Solids*, vol. 198–200, pp. 728–731, May 1996.
- [98] R. A. Street, *Hydrogenated amorphous silicon*. Cambridge: Cambridge university press.
- [99] J. Bardeen, "Surface state and rectification at a metal semi-conductor contact," *Phys. Rev.*, vol. 71, no. 10, pp. 717–727, May 1947.
- [100] W. Monch, "Role of virtual gap states and defects in metal-semiconductor contacts," *Phys. Rev. Lett.*, vol. 58, no. 12, pp. 1260–1263, 1987.
- [101] J. L. Freeouf and J. M. Woodall, "Schottky barriers: An effective work function model," *Appl. Phys. Lett.*, vol. 39, no. 9, pp. 727–729, Nov. 1981.
- [102] L. W. W. Fang, R. Zhao, J. Pan, Z. Zhang, L. Shi, T. C. Chong, and Y. C. Yeo, "Fermi-level pinning at the interface between metals and nitrogen-doped  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  examined by x-ray photoelectron spectroscopy," *Appl. Phys. Lett.*, vol. 95, p. 192109, 2009.
- [103] L. W. W. Fang, J.-S. Pan, R. Zhao, L. Shi, T. C. Chong, G. Samudra, and Y.-C. Yeo, "Band alignment between amorphous  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  and prevalent complementary-metal-oxide-semiconductor materials," *Appl. Phys. Lett.*, vol. 92, p. 032107, 2008.
- [104] L. W. W. Fang, R. Zhao, E. G. Yeo, K. G. Lim, H. Yang, L. Shi, T. C. Chong, and Y. C. Yeo, "Phase change random access memory devices with nickel silicide and platinum silicide electrode contacts for integration with CMOS technology," *J. of The Electrochemical Society*, vol. 158, no. 3, pp. H232–H238, 2011.
- [105] L. W. W. Fang, Z. Zhang, R. Zhao, J. Pan, M. Li, L. Shi, T. C. Chong, and Y. C. Yeo, "Fermi-level pinning and charge neutrality level in nitrogen-doped  $\text{Ge}_2\text{Sb}_2\text{Te}_5$ : Characterization and application in phase change memory devices," *J. Appl. Phys.*, vol. 108, p. 053708, 2010.
- [106] M. Kobayashi, A. Kinoshita, K. Swraswat, H. S. P. Wong, and Y. Nishi, "Fermi-level dipinning in metal-ge schottky junction and its application to metal source drain Ge NMOSFET," in *Dig. Tech. Sympo. VLSI Tech.*, 2008, pp. 54–55.
- [107] T. Nishimura, K. Kita, and A. Toriumi, "Evidence of strong fermi-level pinning due to metal induced gap states at metal-germanium interface," *Appl. Phys. Lett.*, vol. 91, p. 123123, 2007.

- [108] Y. Zhou, Y. W. Wei Han, F. Xiu, J. Zou, R. K. Kawakami, and K. L. Wang, "Investigating the origin of fermi level pinning in Ge schottky junctions using epitaxially grown ultrathin MgO films," *Appl. Phys. Lett.*, vol. 96, p. 102103, 2010.
- [109] Y. Matsui, K. Kurotsuchi, O. Tonomura, T. Morikawa, M. Kinoshita, Y. Fujisaki, N. Matsuzaki, S. Hanzawa, M. Terao, N. Takaura, H. Moriya, T. Iwasaki, M. Moniwa, and T. Koga, "Ta<sub>2</sub>O<sub>5</sub> interfacial layer between GST and W plug enabling low power operation of phase change memories," in *IEDM Tech. Dig.*, Dec. 2006, pp. 1–4.
- [110] J. Robertson, "Band offsets of wide-band-gap oxides and implications for future electronic devices," *J. Vac. Sci. Technol. B*, vol. 18, no. 3, pp. 1785–1791, 2000.
- [111] J. Tersoff, "Band lineup at II-VI hetero-junctions: Failure of the common anion rule," *Phys. Rev. Lett.*, vol. 56, no. 25, pp. 2755–2758, 1986.
- [112] N. F. Mott and R. A. Street, "States in the gap in chalcogenide glasses," *Phys. Rev. Lett.*, vol. 36, pp. 33–52, 1977.
- [113] N. Yamada and T. Matsunaga, "Structure of laser-crystallized Ge<sub>2</sub>Sb<sub>2+x</sub>Te<sub>5</sub> sputtered thin films for use in optical memory," *J. Appl. Phys.*, vol. 88, no. 12, pp. 7020–7028, Dec. 2000.
- [114] L. W. Qu, X. S. Miao, J. J. Shen, Z. Li, J. J. Sun, P. An, J. Huang, D. Yang, and C. Liu, "SET-RESET properties dependence of phase-change memory cell on thickness of phase-change layer," *Solid-State Electronics*, vol. 56, no. 1, pp. 191–195, 2011.
- [115] S. Raoux, J. L. Jordan-Sweet, and A. J. Kellock, "Crystallization properties of ultrathin phase change films," *J. Appl. Phys.*, vol. 103, no. 11, pp. 114310–7, 2008.
- [116] G.-F. Zhou and B. A. J. Jacobs, "High performance media for phase change optical recording," *Jpn. J. Appl. Phys.*, vol. 38, pp. 1625–1628, 1999.
- [117] D. Adler, H. K. Henisch, and S. N. Mott, "The mechanism of threshold switching in amorphous alloys," *Rev. Mod. Phys.*, vol. 50, no. 2, pp. 209–220, Apr. 1978.
- [118] H. Y. Wey, "Surface of amorphous semiconductors and their contacts with metals," *Phys. Rev. B*, vol. 13, pp. 3495–3505, 1976.
- [119] D. K. Reinhard, D. Adler, and F. O. Arntz, "Electron- and photon-induced conductivity in chalcogenide glasses," *J. Appl. Phys.*, vol. 47, no. 4, pp. 1560–1573, 1976.
- [120] R. S. Muller and T. I. Kamins, *Device electronics for integrated circuits*. John Wiley & Sons, Inc., no. 0-471-84309-1, ch. 3.
- [121] N. Takaura, M. Terao, K. Kurotsuchi, T. Yamauchi, O. Tonomura, Y. Hanaoka, R. Take-mura, K. Osada, T. Kawahara, and H. Matsuoka, "A GeSbTe phase-change memory cell featuring a tungsten heater electrode for low-power, highly stable, and short-read-cycle operations," in *IEDM Tech. Dig.*, Dec. 2003, pp. 897–900.
- [122] G. Bruns, P. Merkelbach, C. Schlockermann, M. Salinga, M. Wuttig, T. D. Happ, J. B. Philipp, and M. Kund, "Nanosecond switching in GeTe phase change memory cells," *Appl. Phys. Lett.*, vol. 95, 043108, 2009.
- [123] J. Siegel, A. Schropp, J. Solis, C. N. Afonso, and M. Wuttig, "Rewritable phase-change optical recording in Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> films induced by picosecond laser pulses," *Appl. Phys. Lett.*, vol. 84, no. 1, p. 2250, Mar. 2004.
- [124] A. K. Jonscher, "The role of contacts in frequency-dependent conduction in disordered solids," *J. Phys. C:Solid-state Phys.*, vol. 6, pp. L235–L239, 1973.
- [125] J. Mueller, R. Thoma, E. Demircan, C. Bernicot, and A. Juge, "Modeling of MOSFET parasitic capacitances, and their impact on circuit performance," *Solid-state Elec.*, vol. 51, pp. 1485–1493, 2007.
- [126] E. G. Yeo, L. P. Shi, K. G. L. R. Zhao, T. C. Chong, and I. Adesida, "Parasitic capacitance effect on programming performance of phase change random access memory devices," *Appl. Phys. Lett.*, vol. 96, p. 043506, 2010.

- [127] H. L. Evans, X. Wu, E. S. Yang, and P. S. Ho, "Accurate phase capacitance spectroscopy of transition metal silicon diodes," *Appl. Phys. Lett.*, vol. 46, no. 5, pp. 486–488, Mar. 1985.
- [128] J. Osvald and E. Burian, "C-V dependence of inhomogeneous schottky diodes," *Solid-state Elec.*, vol. 42, no. 2, pp. 191–195, 1998.
- [129] M. C. A. M. Koolen, J. A. M. Geelen, and M. P. J. G. Versleijen, "An improved de-embedding technique for on-wafer high frequency characterization," in *in Proc. IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Sept. 1991, pp. 188–191.
- [130] L. F. Tiemeijer and R. J. Havens, "A calibrated lumped-element de-embedding technique for on-wafer RF characterization of high-quality inductors and high-speed transistors," *IEEE Trans. Electron Devices*, vol. 50, no. 3, pp. 822–829, Mar. 2003.
- [131] J. Luo and D. A. Dornfeld, "Material removal mechanism in chemical mechanical polishing: theory and modeling," *IEEE Trans. Semiconduct. Manufact.*, vol. 14, no. 2, pp. 112–133, May 2001.
- [132] R. Chang, Y. Cao, and C. J. Spanos, "Modeling the electrical effects of metal dishing due to CMP for on-chip interconnect optimization," *IEEE Trans. Electron Devices*, vol. 51, no. 10, pp. 1577–1583, Oct. 2004.
- [133] L. Wuz and C. Yan, "An analytical model for step height reduction in CMP with different pattern densities," *J. Electrochem. Soc.*, vol. 154, no. 7, pp. H596–H603, 2007.
- [134] M. E. Day, M. Delfino, and S. Salimian, "Low energy ion etching of aluminum oxide films and native aluminum oxide," *J. Appl. Phys.*, vol. 72, pp. 5467–5470, Dec. 1992.
- [135] A. M. Goodman, "Metal-semiconductor barrier height measurement by the differential capacitance method-one carrier system," *J. Appl. Phys.*, vol. 34, no. 2, pp. 329–337, Feb. 1963.
- [136] C. D. Wang, C. Y. Zhu, G. Y. Zhang, J. Shen, and L. Li, "Accurate electrical characterization of forward ac behavior of real semiconductor diode: giant negative capacitance and nonlinear interfacial layer," *IEEE Electron Device Lett.*, vol. 50, no. 4, pp. 1145–1147, Apr. 2003.
- [137] E. G. Woelk, H. Krautle, and H. Beneking, "Measurement of low resistive ohmic contacts semiconductors," *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 19–22, Jan. 1986.
- [138] N. Stavitski, M. J. H. van Dal, A. Lauwers, C. Vrancken, A. Y. Kovalgin, and R. A. M. Wolters, "Systematic TLM measurements of NiSi and PtSi specific contact resistance to n- and p-type Si in a broad doping range," *IEEE Electron Device Lett.*, vol. 29, no. 4, pp. 378–381, Apr. 2008.
- [139] S. M. Yoon, K. J. Choi, Y. S. Park, S. Y. Lee, N. Y. Lee, and B. G. Yu, "Dry etching of Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> thin films into nanosized patterns using TiN mask," *Jpn. J. Appl. Phys.*, vol. 45, no. 40, pp. L1080–L1083, 2006.
- [140] S. M. Yoon, N. Y. Lee, S. O. Ryu, Y. S. Park, S. Y. Lee, K. J. Choi, and B. G. Yu, "Etching characteristics of Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> using high-density helicon plasma for the nonvolatile phase-change memory applications," *Jpn. J. Appl. Phys.*, vol. 44, no. 27, pp. L869–L872, 2005.
- [141] L. Stafford, J. Margot, S. Delprat, M. Chaker, and S. J. Pearton, "Influence of redeposition on the plasma etching dynamics," *J. Appl. Phys.*, vol. 101, p. 083303, 2007.
- [142] G. M. Feng, B. Liu, Z. T. Song, S. L. Feng, and B. Chen, "Reactive ion etching of Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> in CHF<sub>3</sub>/O<sub>2</sub> plasma for nonvolatile phase-change memory device," *Electrochem. and Solid-State Lett.*, vol. 10, no. 5, pp. D47–D50, 2007.
- [143] K.-Y. Yang, S.-H. Hong, D. kee Kim, B. ki Cheong, and H. Lee, "Patterning of Ge<sub>2</sub>Sb<sub>2</sub>Te<sub>5</sub> phase change material using uv nano-imprint lithography," *Microelectronic Engineering*, vol. 84, pp. 21–24, 2007.

- 
- [144] N. Stavitski, "Silicide-to-silicon specific contact resistance characterization: test structures and models," Ph.D. dissertation, University of Twente, 2009.
- [145] A. S. Holland, G. K. Reeves, and P. W. Leech, "Universal error corrections for finite semiconductor resistivity in cross-kelvin resistor test structures," *IEEE Electron Device Lett.*, vol. 51, no. 6, pp. 914–919, June 2004.
- [146] S. S. Cohen and G. S. Gildenblat, *Metal-semiconductor contacts and devices: VLSI Electronics Microstructure Science Vol. 13*. London: Academic Press, 1986.
- [147] *PMGI & LOR Under Layer Resists*. [Online]. Available: <http://www.microchem.com/Prod-PMGI-LOR.htm>
- [148] *LOR and PMGI Resists*. [Online]. Available: <http://www.microchem.com/pdf/PMGI-Resists-data-sheetV-rhcredit-102206.pdf>
- [149] S. E. Swirhun, W. M. Loh, R. M. Swanson, and K. Saraswat, "Current crowding effects and determination of specific contact resistivity from contact end resistance (cer) measurements," *IEEE Electron Device Lett.*, vol. 6, pp. 639–641, Dec. 1985.
- [150] V. Heine, "Theory of surface states," *Phys. Rev. A*, vol. 138, no. 6A, pp. A1689–A1696, June 1965.
- [151] D. Roy, M. A. in 't Zandt, and R. A. Wolters, "Specific contact resistance of phase change materials to metal electrodes," *IEEE Electron Device Lett.*, vol. 31, pp. 1293–1295, Nov. 2010.





## Samenvatting

De ontwikkelingen in geïntegreerde schakelingen (IC's) vereisen snellere en goedkope niet-vluchtige geheugens met een betere schaalbaarheid. Geheugens gebaseerd op materialen met een faseovergang (phase change materialen) zijn een goede kandidaat om aan deze eisen te voldoen. Bij het verkleinen van de maatvoering in nieuwe technologieën nemen de (contact)oppervlakken kwadratisch af en de kennis van de eigenschappen van deze contacten wordt steeds belangrijker. Dit proefschrift behandelt de karakterisering van elektrische contacten in dit type geheugens. Het betreft hier in het bijzonder de elektrische contacten binnen een geheugencel, dat wil zeggen de contacten tussen een metaalelektrode en het phase change materiaal in de amorfe en in de kristallijne fase.

De contacten worden gekarakteriseerd door elektrische metingen aan geschikte teststructuren. De waarde ervan wordt gegeven als de contactweerstand ( $R_C$ ) en de specifieke contactweerstand ( $\rho_c$ ). De gebruikte structuren van Kelvinweerstand en overdrachtslengte (transfer length) methode worden in hoofdstuk 2 beschreven. De metingen en berekeningen met deze teststructuren worden behandeld. De vorming van een grenslaag en het mechanisme van ladingsoverdracht over een metaal-halfgeleider contact worden kort samengevat. De meest toegepaste materialen voor phase change geheugens zijn  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  en legeringen van  $\text{Sb}_2\text{Te}$ . De temperatuur van een faseovergang, de elektrische eigenschappen zoals soortelijke weerstand en dichtheid en beweeglijkheid van ladingsdragers en de relevante optische eigenschappen van deze materialen zijn verzameld in hoofdstuk 3. Kennis van deze eigenschappen is van belang voor het maken van teststructuren en het beschrijven van het mechanisme van ladingstransport over contacten van een metaal met deze materialen. De verkregen waarden van de specifieke contactweerstand ( $\rho_c$ ) van verschillende geschikte metaalelektrodes met amorfe en kristallijne phase change materialen worden gegeven in hoofdstuk 4. De vergelijking van

structuren van Kelvinweerstand en de transfer length methode geven vergelijkbare waarden van  $\rho_c$ . In phase change geheugens kunnen lagen van phase change materiaal met een dikte van 5 tot 50 nm gebruikt worden. De verandering van de waarden van  $\rho_c$  voor deze diktes is onderzocht. Voor contacten van amorf phase change materiaal wordt een sterke exponentiële afhankelijkheid met de temperatuur en de aangelegde spanning gemeten. Met behulp van deze meetgegevens en de materiaaleigenschappen kan het mechanisme van ladingsoverdracht over deze contacten beschreven worden met het geldende metaal-halfgeleider contactmodel. In het geval van amorf phase change materiaal is dit thermionische/thermionische veldemissie, terwijl dat voor de kristallijne fase een tunnelmechanisme is. Door gebruik te maken van verschillende metaalelektrodes kan het contact met amorf phase change materiaal beschreven worden met de vorming van een grenslaag door elektrisch positieve en negatieve defecten in het amorfe materiaal.

Normaliter wordt de specifieke contactweerstand bepaald met behulp van elektrische gelijkspanningsmetingen. Het programmeren en lezen van geheugencellen kan voor bepaalde toepassingen met een hoge frequentie gebeuren. In hoofdstuk 5 wordt een nieuwe, aangepaste TLM structuur en bijbehorende berekeningen gegeven, waarmee de contactweerstand ook bij deze hoge frequenties kan worden bepaald. Deze structuren zijn gemaakt en gemeten; de specifieke contactweerstand is bepaald bij frequenties tot 4 MHz.

Het voorkomen van parasitaire weerstanden in teststructuren heeft een grote invloed op de elektrische metingen. Randen van gereponeerd geleidend phase change materiaal, gevormd tijdens het patroneren van de teststructuren, geven additionele geleidende gebieden. Deze beïnvloeden de meting van de vierkantsweerstand van Van der Pauw structuren en van de contactweerstand van Kelvinweerstand. Experimenten om de contactweerstand van amorf naar kristallijn phase change materiaal te bepalen werden nadelig beïnvloed door problemen met het maken en door ongewenste gedeeltelijke kristallisatie van het amorfe materiaal. Transmissie elektronen microscopie lieten het ontstaan van parasitaire weerstanden zien.

Dit proefschrift geeft kennis van contacten van metaalelektrodes met phase change materiaal in de vorm van de waarden van de specifieke contactweerstand en het mechanisme van ladingsoverdracht in deze contacten. Dit is belangrijk voor het ontwerpen, het modelleren en het schalen en optimaliseren van geheugencellen.

## Summary

Advancements in integrated circuits demand an increasing requirement for a faster, low-cost non-volatile memory with improved scaling potential. Phase change memory is an important emerging memory technology qualifying these requirements. With dimensional scaling, the contacts are scaled by  $F^2$ , therefore knowledge of the contact properties becomes even more important. This thesis deals with the characterization of electrical contacts for phase change memory cells. An electrical contact in this respect refers to the interfaces formed in the memory cell, *i.e.* the metal electrode to phase change material (PCM) contacts in the crystalline and in the amorphous state.

The contacts are electrically characterized using dedicated test structures, its value is expressed in terms of contact resistance ( $R_C$ ) and specific contact resistance ( $\rho_c$ ). The different test structures (Kelvin resistor and transfer length method (TLM)) used for contact resistance characterization in this thesis is reviewed in chapter 2. The measurement and the data extraction procedures from these test structures are discussed. Barrier formation and charge transport mechanism at a metal to semiconductor interface is briefly described.

The commonly used PCM for memory applications are  $\text{Ge}_2\text{Sb}_2\text{Te}_5$  and doped- $\text{Sb}_2\text{Te}$ . The amorphous to crystalline transition temperature, electrical properties like resistivity, mobility, carrier concentration and relevant optical properties of both these PCM are given in chapter 3. The knowledge of these parameters is essential for test structure fabrication and modeling of the charge transport mechanism at the electrode to PCM interface.

The  $\rho_c$  values obtained for CMOS compatible electrodes to amorphous and crystalline PCM are provided in chapter 4. Comparison of Kelvin resistor and circular TLM test structures resulted in similar  $\rho_c$  values. Phase change memory technology uses PCM layers in the range from 2.5 nm to 50 nm thickness.

The change in  $\rho_c$  values is studied for amorphous and crystalline PCM layers in this thickness range. For contacts to PCM in the amorphous state, a strong exponential dependence of  $\rho_c$  values with measurement temperature and voltage bias is observed. Based on these measurements and the knowledge of the PCM material parameters, the charge transport mechanism at the metal to PCM interface is validated with a metal-semiconductor model. It turns out that the main charge transport mechanism at the electrode to amorphous PCM interface is thermionic/thermionic field emission, while at the electrode to crystalline PCM interface it is tunneling. Using electrodes with different work function, the interface barrier creation at the metal to amorphous PCM interface is modeled assuming donor like and acceptor like states in the PCM.

The specific contact resistance is commonly extracted from measurements performed at DC current and voltage. Depending on the application, these memory cells may be accessed typically in the MHz range. In chapter 5, a modified TLM structure and a novel data extraction procedure are presented, for contact resistance measurements as a function of frequency. Measurements were performed on these fabricated test structures and  $\rho_c$  values were extracted up to 4 GHz.

The formation of parasitic current paths in test structures significantly affects the electrical resistance measurements. Conducting re-sputtered PCM sidewalls formed during etching result in parasitic current paths that significantly affect the sheet resistance measurements from Van der Pauw structures and contact resistance measurements from Kelvin resistor structures. Experiments performed to characterize the crystalline PCM to amorphous PCM interfaces are hindered by processing limitations and partial crystallization of the PCM. Supporting TEM evidences for parasitic current paths are provided.

This thesis provides a general understanding of electrode to PCM contacts in terms of  $\rho_c$  values and interface charge transport mechanism. The knowledge of this  $\rho_c$  values is essential for design, modeling, scaling and optimization of memory cells.

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## Author biography

Deepu Roy was born on May 28, 1982 in Kerala, India. He received his B. Tech degree in Instrumentation from Cochin University of Science and Technology, Cochin, Kerala, India, in 2004 and M.Sc Degree in Electrical Engineering with specialization in Microelectronics from Technical University Delft, Delft, The Netherlands in 2007.

From 2004 to 2005, he worked as a project engineer at Sophisticated Test and Instrumentation Center (STIC), Cochin, India, where he was involved in the development of a plantar pressure monitoring system. In 2006, as part of his M.Sc programme, he carried out his thesis work at NXP Semiconductors, Eindhoven, The Netherlands, entitled security coating as a Physically Uncloneable Function (PUF). He continued at NXP Semiconductors working towards his Ph.D. degree in collaboration with MESA+ institute of Nanotechnology, Chair of Semiconductor Components, University of Twente, Enschede, The Netherlands. His research work focused on the characterization of electrical contacts for phase change random access memory cells.

This thesis summarizes the major results obtained during his Ph.D. research work.



## List of publications

### Journals

1. Deepu Roy, Johan Klootwijk, Dirk. J. Gravesteijn and Rob Wolters, "Electrode to phase change material interface with donor and acceptor like traps", *IEEE Electron Device Lett.* (In preparation).
2. Deepu Roy, Ralf Pijper, Luuk F. Tiemeijer and Rob A.M. Wolters, "High frequency contact resistance measurements", *IEEE Trans. Semiconductor Manufacturing*, Invited paper (Submitted).
3. Deepu Roy, Micha A.A. in 't Zandt and Rob A.M. Wolters, "Electrical characterization of re-sputtered sidewalls in thin-film structures", *IEEE Trans. Electron Devices*, vol. 58, pp. 924-930, April 2011.
4. Deepu Roy, Micha A.A. in 't Zandt and Rob A.M. Wolters, "Specific contact resistance of phase change materials to metal electrodes", *IEEE Electron Device Lett.*, vol. 31, pp. 1293-1295, Nov 2010.
5. D. Roy, J.H. Klootwijk, N.A.M Verhaegh, H.H.A.J. Roosen and R.A.M. Wolters, "Comb capacitor structures for on-chip physical uncloneable function", *IEEE Trans. Semiconductor Manufacturing*, vol. 22, pp. 96-102, Feb 2009.
6. Deepu Roy and J. Philip, "Total system calibration of a plantar foot pressure measurement unit", *J. Instrument Soc. India*, vol. 36(1) pp. 45-45, 2006.

### Conference proceedings - Oral presentations

1. Deepu Roy, Johan Klootwijk, Dirk. J. Gravesteijn and Rob Wolters, "Contact Resistance of TiW to ultra thin phase change material layers," in *proc. European Solid-State Device Research Conference (ESSDERC)*, Sep 2011 (Accepted).
2. Deepu Roy, Dirk. J. Gravesteijn and Rob A.M. Wolters, "Interface characterization of metals and metal-nitrides to phase change materials", *MRS Spring meeting*, April 2011.
3. Deepu Roy, Ralf Pijper, Luuk F. Tiemeijer and Rob A. M. Wolters, "Contact Resistance Measurement Structures at High Frequencies" in *proc. of 24<sup>th</sup> IEEE International*

- Conference on Microelectronic Test Structures(ICMTS)*, pp. 49-54, Amsterdam, April 2011.
4. K. Attenborough, G.A.M. Hurkx, R. Delhougne, J. Perez, M.T. Wang, T.C. Ong , Luan Tran, D. Roy, D.J. Gravesteijn, M. J. van Duuren, "Phase Change Memory Line Concept for Embedded Memory Applications" in *Tech. Dig. IEEE International Electron Devices Meeting (IEDM)*, Pages: 29.2.1-29.2.4, Dec 2010.
  5. D. Roy , M.A.A. in 't Zandt, C.E. Timmering, J.H. Klootwijk and R.A.M. Wolters, "Contact resistance of phase change materials to TiW electrodes in amorphous and crystalline state" in *Proc. of 10<sup>th</sup> Non-volatile Memory Technology Symposium (NVMTS)*, pp.12-15, Oct 2009, Portland, USA.
  6. D. Roy, J.H. Klootwijk, N.A.M Verhaegh, H.H.A.J. Roosen and R.A.M. Wolters, "Comb Capacitor structures for measurement of post processed layers",in *Proc. of 21<sup>st</sup> International Conference on Microelectronic Test Structures (ICMTS)*, pp. 205-209, March 2008, Edinburgh, UK.
  7. Deepu Roy and J. Philip, "Instrumentation Development for Plantar Foot Pressure Measurement: A New Approach", *International Conference on Biotechnology and Neuroscience*, pp. 29-31, Dec 2004, Cochin, India.

## Conference proceedings - Poster presentations

1. Deepu Roy, M.A.A. in 't Zandt and R.A.M. Wolters, "Bias dependent specific contact resistance of phase change material to metal contacts" in *Proc. of STW.ICT Conference*, pp. 147-149, Nov 2010, Veldhoven, The Netherlands.; *Annual Conference Materials to Innovate Industry and Society*, December 2010, The Netherlands.
2. Deepu Roy, M.A.A. in 't Zandt and R.A.M. Wolters, "Impact of Sidewalls on Electrical characterization" in *Proc. Annual Workshop on Semiconductor Advances for Future Electronics and Sensors (SAFE)*, pp. 105-107, Nov 2009, Veldhoven, The Netherlands.; *Annual Conference Materials to Innovate Industry and Society*, December 2009, The Netherlands.
3. Deepu Roy, Micha in 't Zandt and Rob Wolters, "Characterization of phase change material to TiW electrode contacts", in *Proc. European/Phase Change and Ovonic Symposium (E/PCOS)*, pp. 190-191, Sep 2009, Aachen, Germany.
4. D. Roy , M.A.A. in 't Zandt, R. Delhougne, J.H. Klootwijk and R.A.M. Wolters, "Characterization of interfaces between electrodes and phase change materials" *Annual Conference Materials to Innovate Industry and Society*, Dec 2008, The Netherlands.
5. D. Roy, M.A.A. in 't Zandt, R. Delhougne, J.H. Klootwijk, R.A.M. Wolters, "Influence of interfacial layer on contact resistance" in *Proc. of Annual Workshop on Semiconductor Advances for Future Electronics and Sensors (SAFE)*, pp. 499-500, Nov 2008, Veldhoven, The Netherlands.

## List of symbols and abbreviations

Table A.2: List of abbreviations

Abbreviations	Explanation
CBKR	Cross Bridge Kevin Resistor
CMP	Chemical Mechanical Polishing
F	Feature size or technology node of semiconductor devices
GSG	Ground Signal Ground
PCM	Phase Change Materials
PCRAM	Phase Change Random Access Memory
SEM	Scanning Electron Microscope
TEM	Transmission Electron Microscope
RIE	Reactive Ion Etching
I-V	Current Voltage (measurements/characteristics)
K	Kelvin
Hz	Hertz
HF	High Frequency
DC	Direct current

Table A.3: List of constants

Constant	Explanation	unit
$q$	Elementary charge	$1.6 \times 10^{-19}$ C
$\epsilon_0$	Permittivity in vacuum	$8.85 \times 10^{-14}$ F/cm
$k_b$	Boltzmann's constant	$1.38 \times 10^{-23}$ J/K
$h$	Planck's constant	$6.626 \times 10^{-34}$ J.s
$c$	speed of light in vacuum	$3 \times 10^8$ m/s

Table A.4: List of symbols

Symbol	Explanation	unit
$\rho_c$	Electrode to PCM specific contact resistance	$\Omega.\text{cm}^2$
$\rho_{CP}$	crystalline PCM to amorphous PCM specific contact resistance	$\Omega.\text{cm}^2$
$\phi_I$	Implantation dose	atoms/cm <sup>2</sup>
$\phi_b$	Barrier height	eV
$\Phi_M$	Metal work function	eV
$\chi$	Electron affinity	eV
$\sigma$	Electrical conductivity	S/m
$\rho$	Electrical resistivity	$\Omega.\text{cm}$
$\mu$	Carrier mobility	cm <sup>2</sup> /V.s
$v$	Charge carrier instantaneous velocity	m/s

Table A.5: List of symbols

Symbol	Explanation	unit
$A$	Area	$\text{cm}^2$ or $\mu\text{m}^2$
$C_D$	Space charge capacitance	$\text{F}/\text{cm}^2$
$D$	Diameter	$\text{cm}$ or $\mu\text{m}$
$I$	Current	A
$L_i$	Length of the metal segment in a Scott TLM structure	$\mu\text{m}$
$l$	Contact transfer length	$\mu\text{m}$
$R_C$	Contact resistance(metal to PCM)	$\Omega$
$R_{CP}$	Crystalline PCM to amorphous PCM contact resistance	$\Omega$
$R_{CT}$	Total contact resistance	$\Omega$
$R_P$	Resistance of the (crystalline) PCM layer	$\Omega$
$R_{PA}$	Resistance of the amorphous PCM layer	$\Omega$
$R_{SH}$	Sheet resistance of PCM layer	$\Omega/\square$
$R_T$	Total resistance of the structure	$\Omega$
$R_K$	Measured resistance of Kelvin resistor structure	$\Omega$
$f_C$	Cutoff frequency	Hz
$f_L$	Minimum frequency	Hz
$J$	Current density	$\text{A}/\text{cm}^2$
$W$	Width of the PCM layer	$\mu\text{m}$
$N_C$	Carrier concentration	$\text{atoms}/\text{cm}^3$
$F_L$	Lorentz force	N
$B$	Magnetic Field Strength	T
$E$	Electric field	$\text{V}/\text{m}$
$E_A$	Activation energy	eV
$E_F$	Fermi energy	eV
$E_P$	Photon energy	eV
$E_g$	Electrical band gap	eV
$E_g^{\text{opt}}$	Optical band gap	eV
$V$	Voltage	V
$V_H$	Hall voltage	V
$R_H$	Hall coefficient	$\text{cm}^3/\text{C}$
$h$	Layer thickness	$\mu\text{m}^2$ or nm
$S$	Edge length of a square van der Pauw structure	$\mu\text{m}^2$
$t$	Time	seconds
$d$	Spacing between the contacts for a TLM structure	$\mu\text{m}$
$V_{TH}$	Threshold switching voltage for amorphous PCM	V

